

8-Bit Parallel-in, Serial-out Shift Register

1 FEATURES

- 8-bit parallel-in, serial-out shift
- Power-Supply Range: 1.65V to 5.5V
- High-current output drive $\pm 10\text{mA}$ @ 5V
- Low Power Consumption: $8\mu\text{A}(\text{Max})$
- Low Input Current: $1\mu\text{A}(\text{Max})$
- Gated Serial Data Input
- Asynchronous Master Reset
- Extended Temperature: -40°C to $+125^\circ\text{C}$

2 APPLICATIONS

- Video Display Systems
- Programmable Logic Controllers
- Enterprise and Communicatios
- Industrial
- Appliances
- LED Displays
- Output Expander

3 DESCRIPTIONS

The RS165 is 8-bit serial or parallel-in/serial-out shift registers. The device features a serial data input (SER), eight parallel data inputs (D0 to D7) and two complementary serial outputs (Q7 and $\overline{Q7}$). When the parallel load input (\overline{PL}) is Low the data from D0 to D7 is loaded into the shift register asynchronously. When \overline{PL} is High data enters the register serially at SER. When the clock enable input (\overline{CE}) is Low data is shifted on the Low-to-High transitions of the CLK input. A High on \overline{CE} will disable the CLK input. Inputs are overvoltage tolerant to 15 V. This enables the device to be used in High-to-Low level shifting applications.

Device Information ⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|---------|-----------------|
| RS165 | TSSOP16 | 5.00mm×4.40mm |
| | SOP16 | 9.90mm×3.90mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Functional Block Diagram

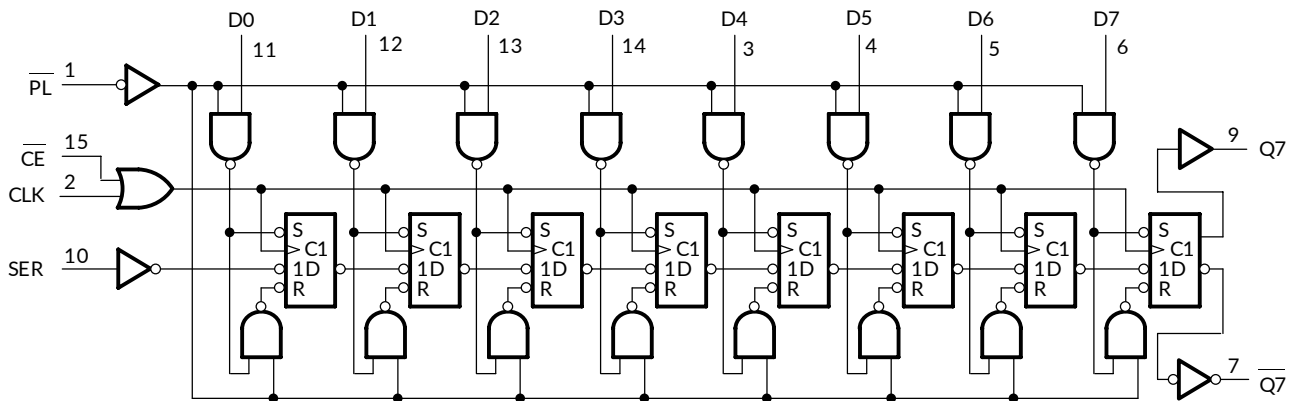


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5 Revision History

Note: Page numbers for previous revisions may differ from page numbers in the current version.

| VERSION | Change Date | Change Item |
|---------|-------------|---------------------------|
| A.1 | 2023/11/03 | Initial version completed |
| A.1.1 | 2024/02/29 | Modify packaging naming |

6 PACKAGE/ORDERING INFORMATION (1)

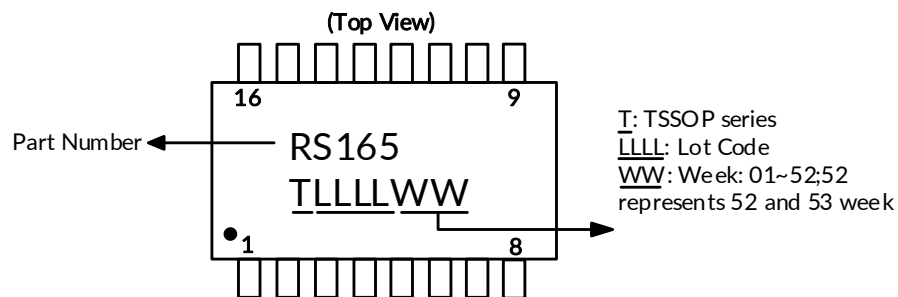
| PRODUCT | ORDERING NUMBER | TEMPERATURE RANGE | PACKAGE LEAD | PACKAGE MARKING (2) | MSL (3) | PACKAGE OPTION |
|---------|-----------------|-------------------|--------------|---------------------|---------|--------------------|
| RS165 | RS165XTSS16 | -40°C ~+125°C | TSSOP16 | RS165 | MSL3 | Tape and Reel,4000 |
| | RS165XS16 | -40°C ~+125°C | SOP16 | RS165 | MSL3 | Tape and Reel,4000 |

NOTE:

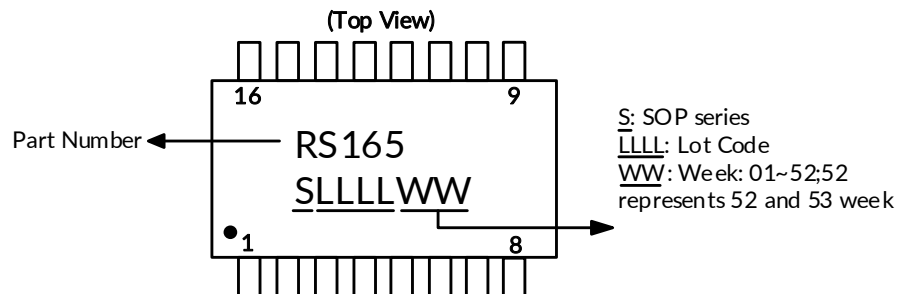
- (1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.
- (2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.
- (3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

Marking Information

(1) TSSOP16

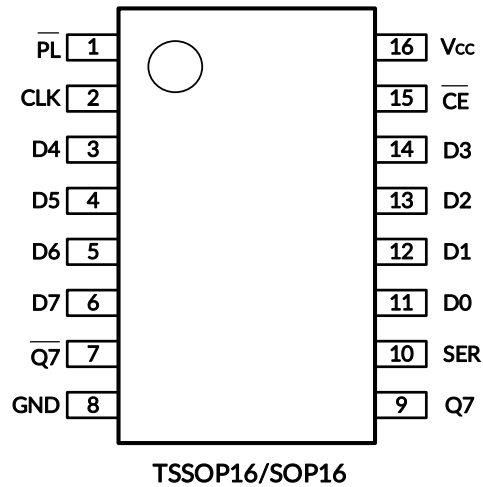


(2) SOP16



7 PIN CONFIGURATIONS

(TOP VIEW)



PIN DESCRIPTION

| PIN | NAME | TYPE ⁽¹⁾ | FUNCTION |
|---------------------|------------------------|---------------------|---|
| TSSOP16/SOP16 | | | |
| 1 | $\overline{\text{PL}}$ | - | Asynchronous parallel load input (active Low) |
| 2 | CLK | I | Clock input (Low-to-High, edge-triggered) |
| 11,12,13,14,3,4,5,6 | D0~D7 | O | Parallel data inputs |
| 7 | $\overline{\text{Q7}}$ | O | Complementary output from the last stage |
| 8 | GND | G | Ground. |
| 9 | Q7 | O | Serial output from the last stage |
| 10 | SER | I | Serial data input |
| 15 | $\overline{\text{CE}}$ | I | Clock enable input (active Low) |
| 16 | V _{CC} | P | Supply voltage |

(1) I=input, O=output, P=power, G=Ground.

8 Functional Table

| Operating modes | Input | | | | | Qn register | | Output | |
|----------------------|------------------------|------------------------|-----|-----|----------|-------------|----------|--------|------------------------|
| | $\overline{\text{PL}}$ | $\overline{\text{CE}}$ | CLK | SER | D0 to D7 | Q0 | Q1 to Q6 | Q7 | $\overline{\text{Q7}}$ |
| Parallel load | L | X | X | X | L | L | L to L | L | H |
| | L | X | X | X | H | H | H to H | H | L |
| Serial shift | H | L | ↑ | l | X | L | q0 to q5 | q6 | $\overline{\text{q6}}$ |
| | H | L | ↑ | h | X | H | q0 to q5 | q6 | $\overline{\text{q6}}$ |
| | H | ↑ | L | l | X | L | q0 to q5 | q6 | $\overline{\text{q6}}$ |
| | H | ↑ | L | h | X | H | q0 to q5 | q6 | $\overline{\text{q6}}$ |
| Hold "Do nothing" | H | H | X | X | X | q0 | q1 to q6 | q7 | $\overline{\text{q7}}$ |
| | H | X | H | X | X | q0 | q1 to q6 | q7 | $\overline{\text{q7}}$ |

H = High voltage level;

h = High voltage level one set-up time prior to the Low-to-High clock transition;

L = Low voltage level;

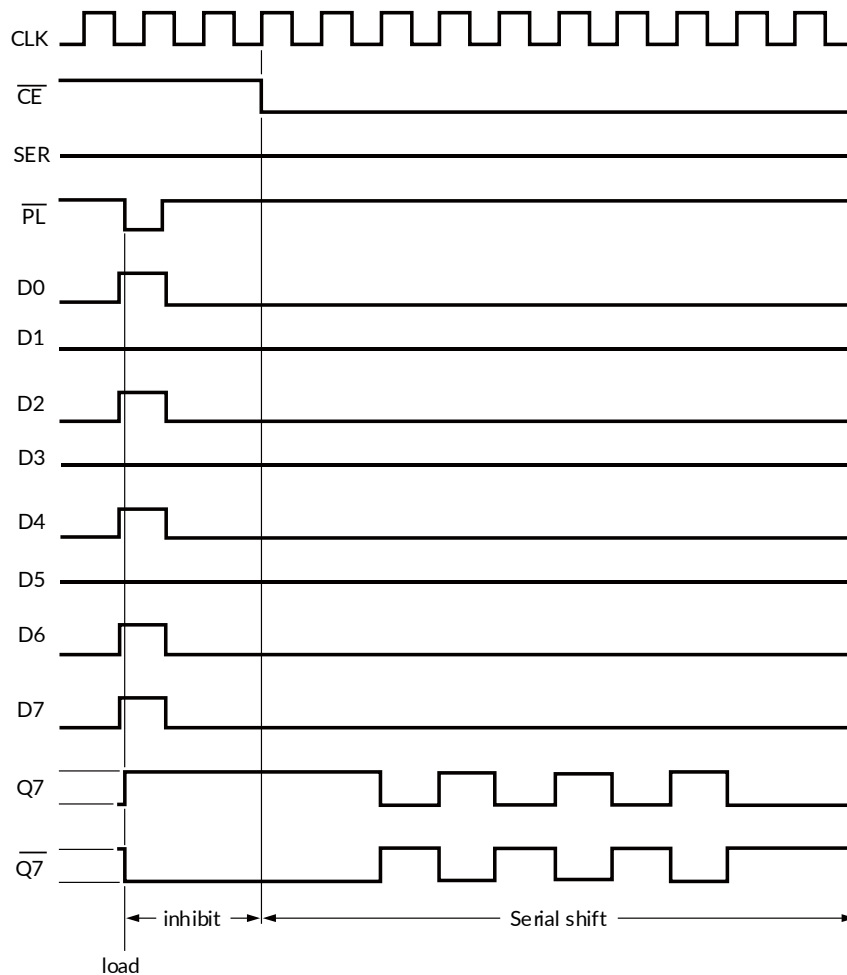
l = Low voltage level one set-up time prior to the Low-to-High clock transition;

q = Lower case letters indicate the state of the referenced input one set-up time prior to the Low-to-High clock transition;

↑ = Low-to-High clock transition;

X = don't care;

8.1 TIMING DIAGRAM



9 SPECIFICATIONS

9.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

| SYMBOL | PARAMETER | CONDITION | MIN | MAX | UNIT |
|------------------|--|---|------|-----|------|
| V _{CC} | Supply Voltage Range | | -0.5 | 6.5 | V |
| I _{IK} | Input Clamp Current | V _I < -0.5 V or V _I > V _{CC} + 0.5 V | | ±20 | mA |
| I _{OK} | Output Clamp Current | V _O < -0.4V or V _O > V _{CC} +0.4V | | ±20 | mA |
| I _O | Output Current | -0.5 V < V _O < V _{CC} + 0.5 V | | ±25 | mA |
| I _{CC} | Supply Current | | | 50 | mA |
| I _{GND} | Ground Current | | -50 | | mA |
| θ _{JA} | Package thermal impedance ⁽²⁾ | TSSOP16 | | 45 | °C/W |
| | | SOP16 | | 150 | |
| T _J | Junction Temperature ⁽³⁾ | | -40 | 150 | °C |
| T _{stg} | Storage Temperature | | -65 | 150 | |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The package thermal impedance is calculated in accordance with JESD-51.

(3) The maximum power dissipation is a function of T_{J(MAX)}, R_{θJA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} - T_A) / R_{θJA}. All numbers apply for packages soldered directly onto a PCB.

9.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

| | | | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), MIL-STD-883K METHOD 3015.9 | ±2000 | V |
| | | Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018 | ±1000 | |
| | | Machine Model (MM), JESD22-A115C (2010) | ±200 | |



ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.3 Recommended Operating Conditions

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------------|---------------------------------|------|-----|-----------------|------|
| Supply voltage | V _{CC} | | 1.65 | | 5.5 | V |
| Input voltage | V _I | | 0 | | V _{CC} | V |
| Output voltage | V _O | | 0 | | V _{CC} | V |
| Input transition rise or fall rate($\Delta t/\Delta v$) | Data inputs | V _{CC} =1.65V to 1.95V | | | 20 | ns/V |
| | | V _{CC} =2.3V to 2.7V | | | 20 | |
| | | V _{CC} =3V to 3.6V | | | 10 | |
| | | V _{CC} =4.5V to 5.5V | | | 5 | |
| Operating temperature | T _A | | -40 | | 125 | °C |

9.4 ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | V _{CC} | TEMP | MIN ⁽¹⁾ | TYP ⁽²⁾ | MAX ⁽¹⁾ | UNIT |
|---------------------------|------------------|--|-----------------|------|-----------------------|--------------------|-----------------------|------|
| High-level input voltage | V _{IH} | | 1.65V to 1.95V | 25°C | 0.65xV _{CC1} | | | V |
| | | | 2.3V to 2.7V | | 1.7 | | | |
| | | | 3V to 3.6V | | 2 | | | |
| | | | 4.5V to 5.5V | | 0.7xV _{CC1} | | | |
| Low-level input voltage | V _{IL} | | 1.65V to 1.95V | 25°C | | | 0.35xV _{CC1} | V |
| | | | 2.3V to 2.7V | | | | 0.7 | |
| | | | 3V to 3.6V | | | | 0.8 | |
| | | | 4.5V to 5.5V | | | | 0.3xV _{CC1} | |
| High-level output voltage | V _{OH} | I _{OH} = -100μA | 1.65V to 5.5V | 25°C | V _{CC} -0.1 | | | V |
| | | I _{OH} = -4mA | 3V | | 1.2 | | | |
| | | I _{OH} = -8mA | 3.3V | | 1.9 | | | |
| | | I _{OH} = -10mA | 5.0V | | 3.8 | | | |
| Low-level output voltage | V _{OL} | I _{OL} = 100μA | 1.65V to 5.5V | 25°C | | | 0.1 | V |
| | | I _{OL} = 4mA | 3V | | | | 0.45 | |
| | | I _{OL} = 8mA | 3.3V | | | | 0.3 | |
| | | I _{OL} = 10mA | 5.0V | | | | 0.4 | |
| Input leakage Current | I _I | V _I =5.5V or GND | 0V to 5.5V | 25°C | | ±0.1 | ±1 | μA |
| | | | | FULL | | | ±5 | |
| | I _{off} | V _I or V _O =5.5V | 0 | 25°C | | ±0.1 | ±1 | μA |
| | | | | FULL | | | ±10 | |
| Supply current | I _{CC} | V _I =5.5V or GND; I _O =0 | 1.65V to 5.5V | 25°C | | 0.1 | 8 | μA |
| | | | | FULL | | | 160 | |
| | ΔI _{CC} | One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND | 3V to 5.5V | FULL | | | 500 | μA |
| Input capacitance | C _I | f=1MHZ | 3.3V | 25°C | | 3.7 | | pF |

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

9.5 Switching Characteristics

| Symbol | PARAMETER | -40°C to +125°C (TYP @25°C) | | | | | | | | | | | | UNIT |
|------------------|---|-----------------------------|-----|-----|----------------------------|-----|-----|----------------------------|------|-----|---------------------------|-----|-----|------|
| | | V _{CC} =1.8V±0.15V | | | V _{CC} =2.5V±0.2V | | | V _{CC} =3.3V±0.3V | | | V _{CC} =5V±0.5 V | | | |
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| t _{pd} | Propagation delay CLK or \overline{CE} to Q7 or $\overline{Q7}$ ⁽¹⁾ | | 44 | | | 20 | | | 14 | | | 9 | | ns |
| | Propagation delay D7 to Q7 or $\overline{Q7}$ | | 29 | | | 17 | | | 12 | | | 9 | | ns |
| | Propagation delay \overline{PL} to Q7 or $\overline{Q7}$ | | 32 | | | 17 | | | 12 | | | 8 | | ns |
| t _t | Transition time Q7 or $\overline{Q7}$ output ⁽²⁾ | | 19 | | | 10 | | | 8 | | | 6 | | ns |
| | t _w Pulser width | | 30 | | | 25 | | | 20 | | | 20 | | ns |
| t _h | Hold width SER to CLK or \overline{CE} | | -12 | | | -5 | | | -5 | | | -3 | | ns |
| | Hold width Dn to \overline{PL} | | -5 | | | -5 | | | -1.5 | | | -1 | | ns |
| | Set-up time SER to CLK or \overline{CE} | | 11 | | | 5 | | | 5 | | | 3 | | ns |
| t _{su} | Set-up time Dn to \overline{PL} | | 5 | | | 5 | | | 1.5 | | | 1 | | ns |
| | t _{REC} Recovery time \overline{PL} to CLK or \overline{CE} | | 5 | | | 1.5 | | | 1 | | | 1 | | ns |
| f _{max} | Maximum frequency For CLK CL=15pF | | 4 | | | 10 | | | 20 | | | 30 | | MHz |

NOTE:

- (1) t_{pd} is the same as t_{PHL} and t_{PLH}.
 (2) t_t is the same as t_{THL} and t_{TLH}.

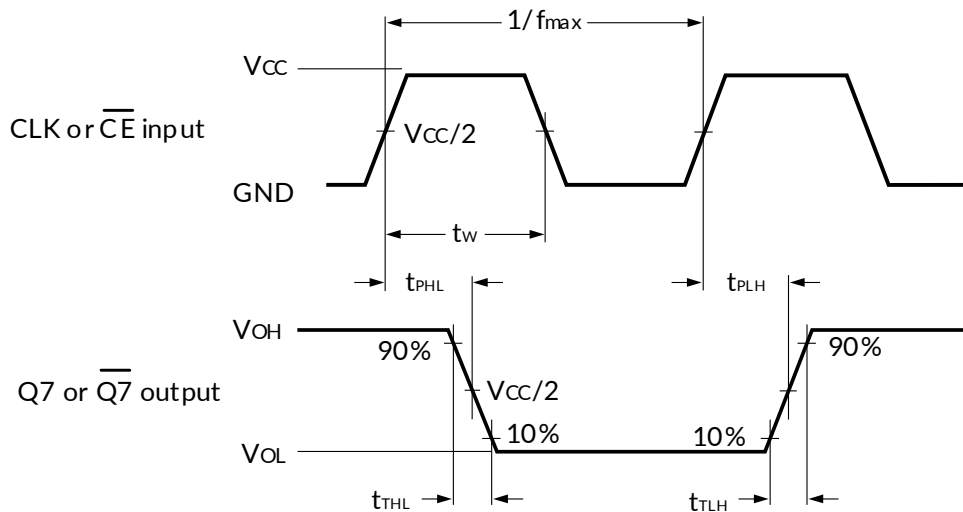
9.6 Operating Characteristics

T_A=25°C

| PARAMETER | TEST CONDITIONS | V _{CC} =3.3V | V _{CC} =5V | UNIT |
|--------------------------------|----------------------------|-----------------------|---------------------|------|
| | | TYP | TYP | |
| C _{pd} ⁽¹⁾ | C _L =0, f=10MHz | 11 | 17 | pF |

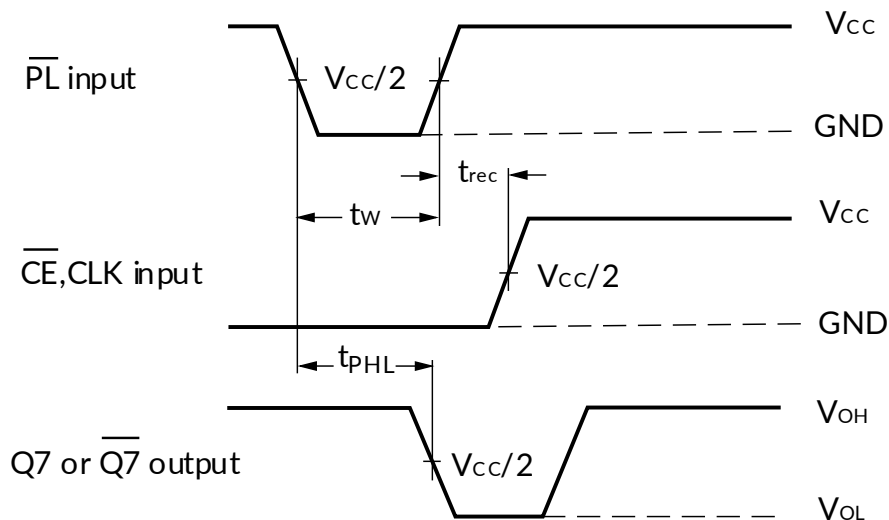
- (1) Power dissipation capacitance per transceiver.

10 Parameter Measurement Information



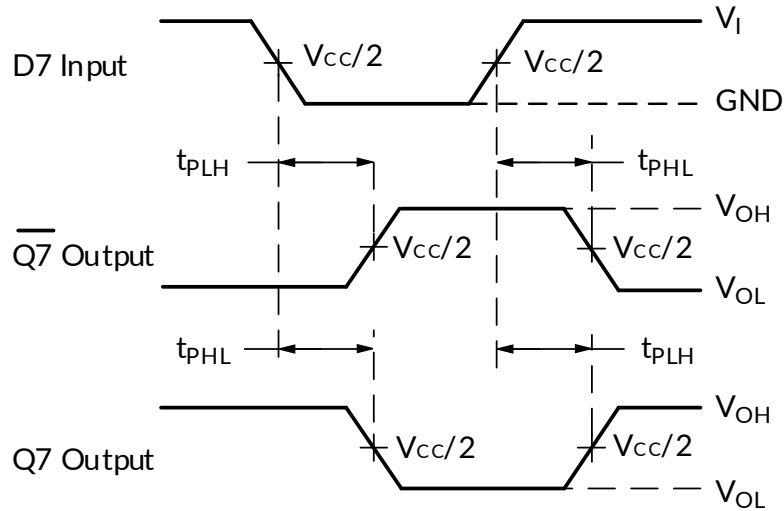
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 1. The clock (CLK) or clock enable (\overline{CE}) to output (Q7 or $\overline{Q7}$) propagation delays, the clock pulse width, the maximum clock frequency and the output transition times



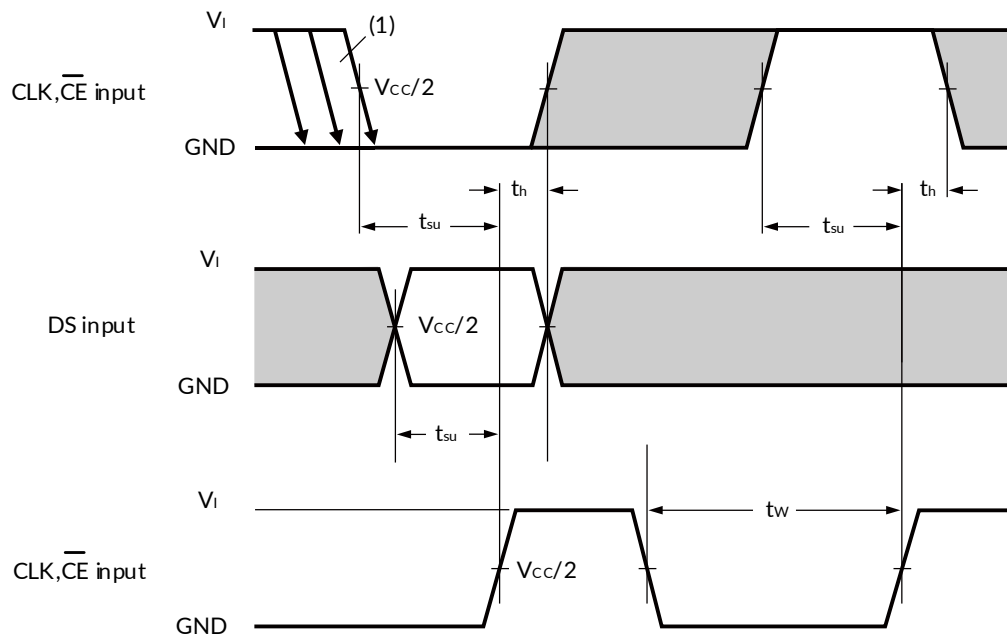
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 2. The parallel load (\overline{PL}) pulse width, the parallel load to output (Q7 or $\overline{Q7}$) propagation delays, the parallel load to clock (CLK) and clock enable (\overline{CE}) recovery time



V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 3. The data input (D7) to output (Q7 or $\overline{Q7}$) propagation delays when \overline{PL} is LOW

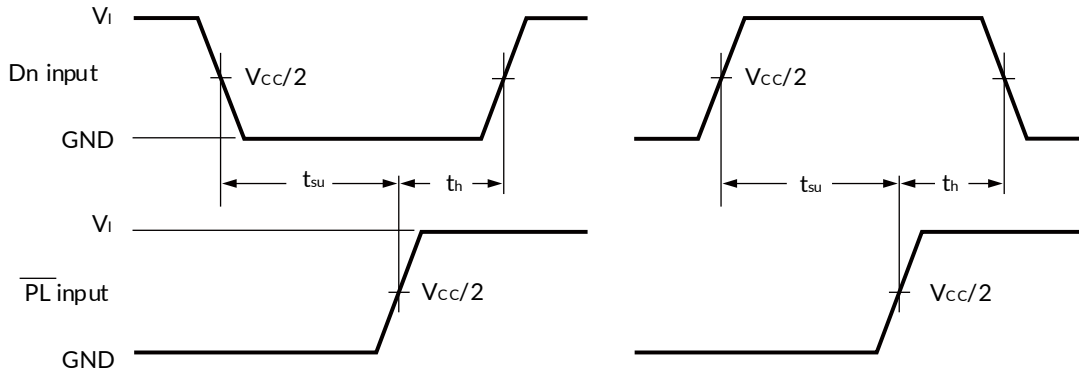


The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

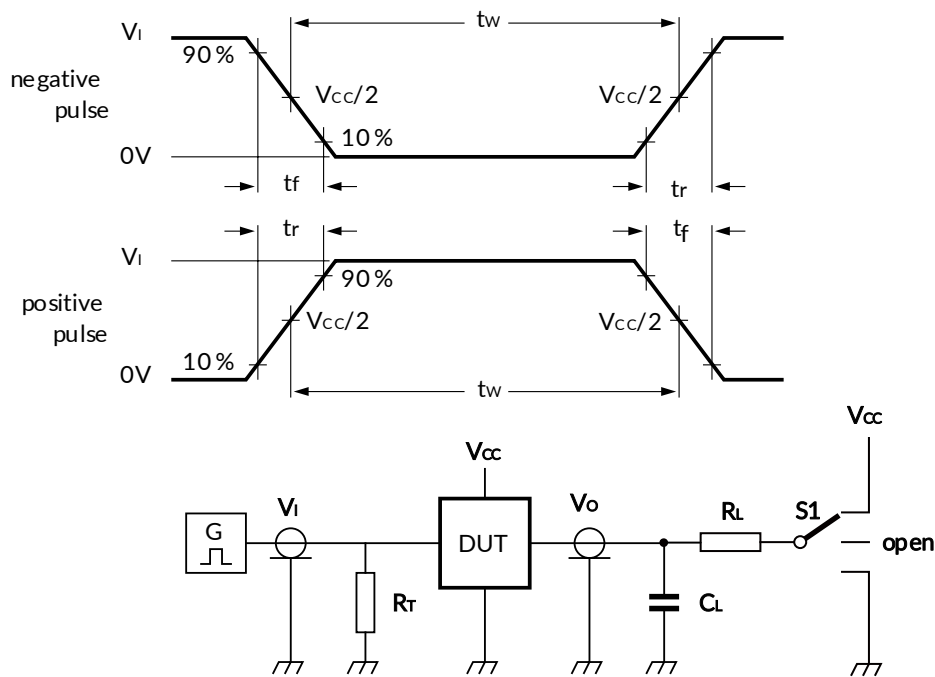
(1) \overline{CE} may change only from HIGH-to-LOW while CLK is LOW, see Section 1.

Figure 4. The set-up and hold times from the serial data input (DS) to the clock (CLK) and clock enable (\overline{CE}) inputs, from the clock enable input (\overline{CE}) to the clock input (CLK) and from the clock input (CLK) to the clock enable input (\overline{CE})



V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 5. The set-up and hold times from the data inputs (Dn) to the parallel load input (PL)



Test data is given in Table 1.

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

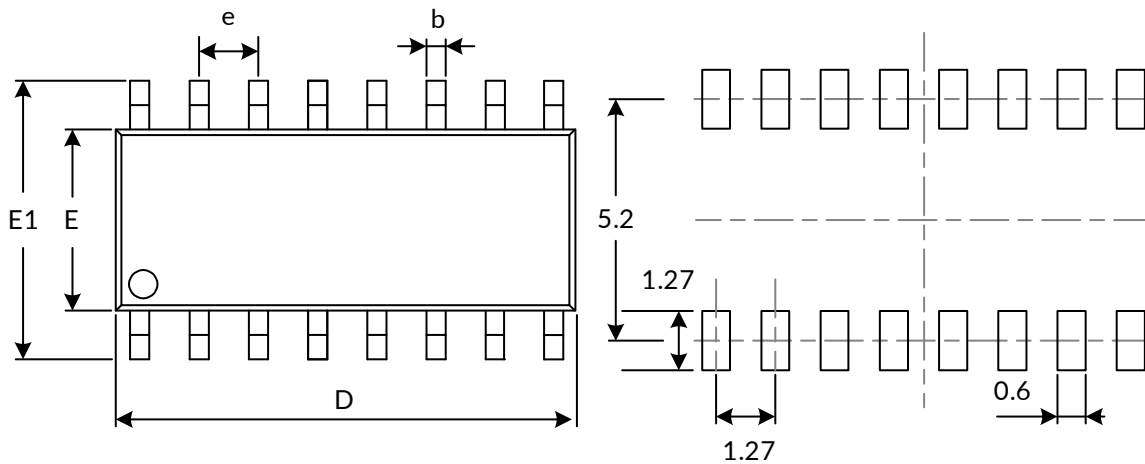
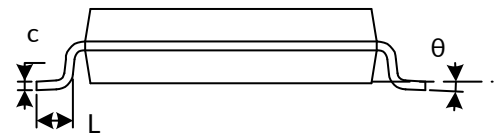
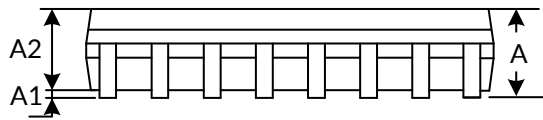
Figure 6. Test circuit for measuring switching times

Table 1. Test data

| S1 position | Input | | Load | |
|-------------------|----------|------------|------------|-------|
| t_{PHL}/t_{PLH} | V_i | t_r, t_f | C_L | R_L |
| open | V_{CC} | 6ns | 15pF, 50pF | 1kΩ |

11 PACKAGE OUTLINE DIMENSIONS

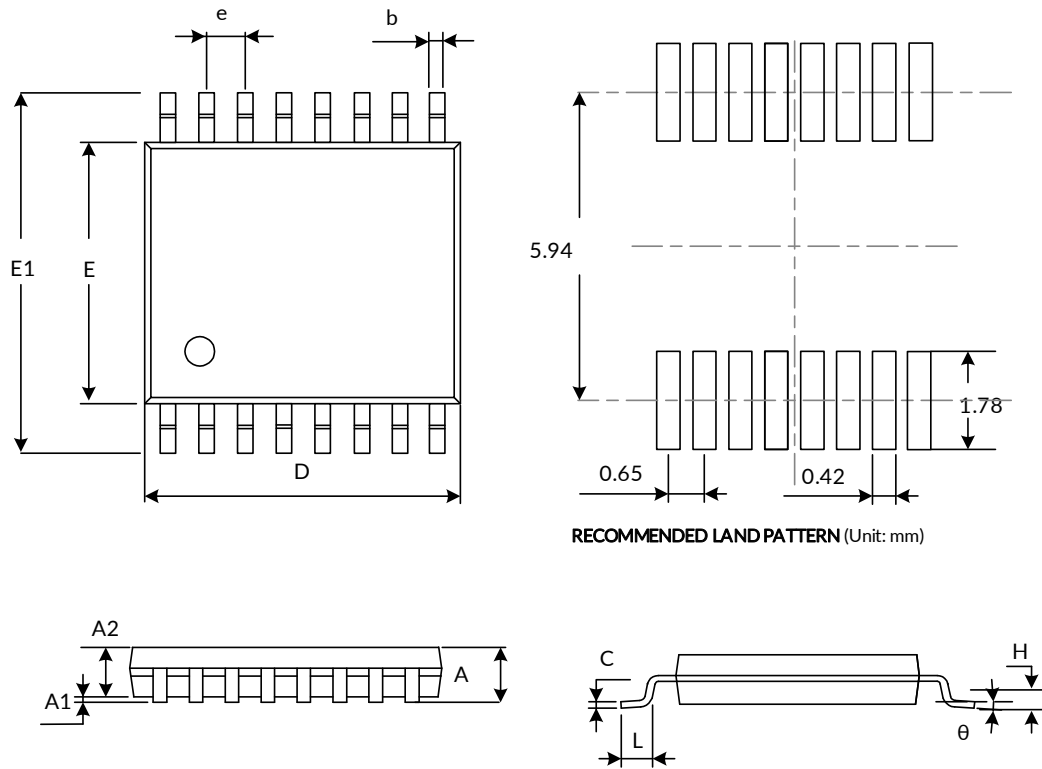
SOP16⁽³⁾


RECOMMENDED LAND PATTERN (Unit: mm)


| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|------------------|----------------------------|-------|----------------------------|-------|
| | Min | Max | Min | Max |
| A ⁽¹⁾ | | 1.750 | | 0.069 |
| A1 | 0.100 | 0.225 | 0.004 | 0.009 |
| A2 | 1.300 | 1.500 | 0.051 | 0.059 |
| b | 0.390 | 0.470 | 0.015 | 0.019 |
| c | 0.200 | 0.240 | 0.007 | 0.010 |
| D ⁽¹⁾ | 9.800 | 10.00 | 0.386 | 0.394 |
| E ⁽¹⁾ | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.200 | 0.228 | 0.244 |
| e | 1.270 (BSC) ⁽²⁾ | | 0.050 (BSC) ⁽²⁾ | |
| L | 0.500 | 0.800 | 0.020 | 0.032 |
| θ | 0° | 8° | 0° | 8° |

NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

TSSOP16 (3)

RECOMMENDED LAND PATTERN (Unit: mm)

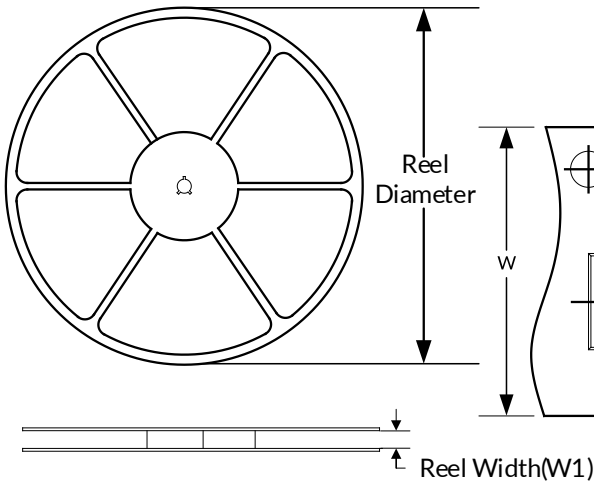
| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|------------------|---------------------------|-------|---------------------------|-------|
| | Min | Max | Min | Max |
| A ⁽¹⁾ | | 1.200 | | 0.047 |
| A1 | 0.050 | 0.150 | 0.002 | 0.006 |
| A2 | 0.900 | 1.050 | 0.035 | 0.041 |
| b | 0.200 | 0.280 | 0.007 | 0.011 |
| c | 0.130 | 0.170 | 0.005 | 0.007 |
| D ⁽¹⁾ | 4.900 | 5.100 | 0.193 | 0.201 |
| E ⁽¹⁾ | 4.300 | 4.500 | 0.169 | 0.177 |
| E1 | 6.200 | 6.600 | 0.244 | 0.260 |
| e | 0.650(BSC) ⁽²⁾ | | 0.026(BSC) ⁽²⁾ | |
| L | 0.450 | 0.750 | 0.017 | 0.030 |
| H | 0.250 TYP | | 0.010 TYP | |
| θ | 0° | 8° | 0° | 8° |

NOTE:

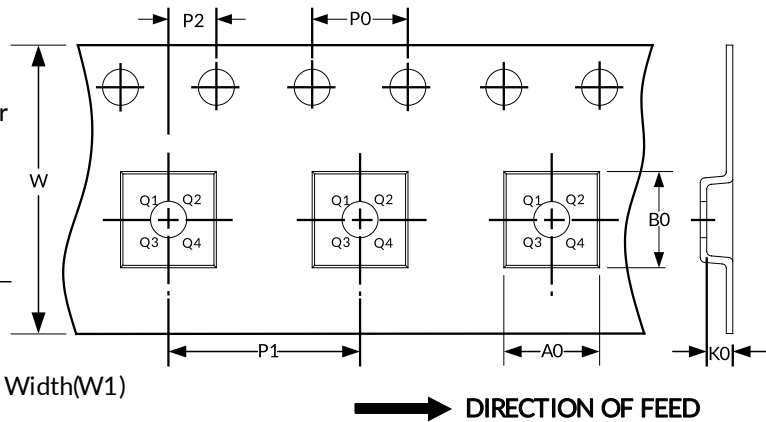
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

12 TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|--------------|---------------|-----------------|---------|---------|---------|---------|---------|---------|--------|---------------|
| SOP16 | 13" | 16.4 | 6.50 | 10.30 | 2.10 | 4.0 | 8.0 | 2.0 | 16.0 | Q1 |
| TSSOP16 | 13" | 12.4 | 6.90 | 5.60 | 1.20 | 4.0 | 8.0 | 2.0 | 12.0 | Q1 |

NOTE:

1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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