

RS7266 Quadruple 2-Input XNOR Gates

1 FEATURES

- **Buffered inputs**
- **Operating Voltage Range: 1.65V to 5.5V**
- **Operating Temperature Range:**
-40°C to +125°C
- **Inputs Accept Voltage to 5.5V**
- **PACKAGES: SOP14 and TSSOP14**

2 APPLICATIONS

- **Detect phase differences in input signals**
- **Create a selectable inverter / buffer**

3 DESCRIPTIONS

This device contains four independent 2-input XNOR gates. Each gate performs the Boolean function $Y = A \oplus B$ in positive logic.

The RS7266 is available in Green SOP14 and TSSOP14 packages. It operates over an ambient temperature range of -40°C to +125°C.

Device Information ⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS7266	SOP14	8.60mm×3.85mm
	TSSOP14	5.00mm×4.40mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Table of Contents

1 FEATURES	1
2 APPLICATIONS	1
3 DESCRIPTIONS	1
4 Revision History	3
5 PACKAGE/ORDERING INFORMATION ⁽¹⁾	4
6 PIN CONFIGURATIONS	5
7 SPECIFICATIONS	6
7.1 Absolute Maximum Ratings	6
7.2 ESD Ratings	6
8 ELECTRICAL CHARACTERISTICS	7
8.1 Recommended Operating Conditions	7
8.2 DC Characteristics	8
8.3 Switching Characteristics	8
8.4 Operating Characteristics	8
9 Parameter Measurement Information	9
10 Detailed Description	10
10.1 Overview	10
10.2 Functional Block Diagram	10
10.3 Device Functional Modes	10
11 Application and Implementation	11
11.1 Application Information	11
11.2 Typical Application	11
12 Power Supply Recommendations	11
13 Layout	12
13.1 Layout Guidelines	12
13.2 Layout Example	12
14 PACKAGE OUTLINE DIMENSIONS	13
15 TAPE AND REEL INFORMATION	15

4 Revision History

Note: Page numbers for previous revisions may differ from page numbers in the current version.

Version	Change Date	Change Item
A.1	2023/09/18	Initial version completed
A.1.1	2024/02/29	Modify packaging naming

5 PACKAGE/ORDERING INFORMATION ⁽¹⁾

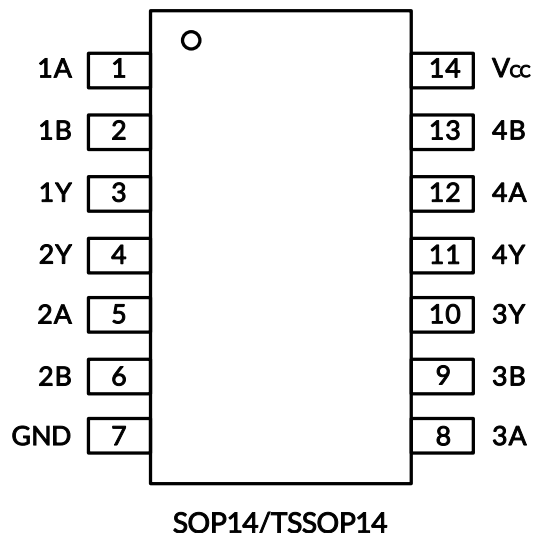
PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING ⁽²⁾	MSL ⁽³⁾	PACKAGE OPTION
RS7266	RS7266XP	-40°C ~+125°C	SOP14	RS7266	MSL3	Tape and Reel,4000
	RS7266XQ	-40°C ~+125°C	TSSOP14	RS7266	MSL3	Tape and Reel,4000

NOTE:

- (1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.
- (2) There may be additional marking, which relates to the lot trace code information(data code and vendor code), the logo or the environmental category on the device.
- (3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

6 PIN CONFIGURATIONS

TOP VIEW



PIN DESCRIPTION

PIN	NAME	I/O ⁽¹⁾	FUNCTION
SOP14/TSSOP14			
1	1A	I	Channel 1 input
2	1B	I	Channel 1 input
3	1Y	O	Channel 1 output
4	2Y	O	Channel 2 output
5	2A	I	Channel 2 input
6	2B	I	Channel 2 input
7	GND	G	Ground
8	3A	I	Channel 3 input
9	3B	I	Channel 3 input
10	3Y	O	Channel 3 output
11	4Y	O	Channel 4 output
12	4A	I	Channel 4 input
13	4B	I	Channel 4 input
14	Vcc	P	Power Supply

(1) I=input, O=output, P=power, G= Ground.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	6.5	V
V _I	Input voltage range ⁽²⁾	-0.5	6.5	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	6.5	V
V _O	Voltage range applied to any output in the high or low state ^{(2) (3)}	-0.5	V _{CC} +0.5	V
I _{IK}	Input clamp current	V _I <0	-50	mA
I _{OK}	Output clamp current	V _O <0	-50	mA
I _O	Continuous output current		±50	mA
	Continuous current through V _{CC} or GND		±100	mA
θ _{JA}	Package thermal impedance ⁽⁴⁾	SOP14	105	°C/W
		TSSOP14	90	
T _J	Junction temperature ⁽⁵⁾	-65	150	°C
T _{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the Recommended Operating Conditions table.

(4) The package thermal impedance is calculated in accordance with JESD-51.

(5) The maximum power dissipation is a function of T_{J(MAX)}, R_{θJA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} - T_A) / R_{θJA}. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

		VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human-body model (HBM), MIL-STD-883K METHOD 3015.9	±2000	V
		Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±1000	V
		Machine Model (MM), JESD22-A115C (2010)	±200	V



ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8 ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (TYP values are at $T_A = +25^{\circ}\text{C}$, Full= -40°C to 125°C , unless otherwise noted.)⁽¹⁾

8.1 Recommended Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Supply voltage	V_{CC}	Operating	1.65	5.5	V
High-level input voltage	V_{IH}	$V_{CC}=1.65\text{V to }1.95\text{V}$	$0.65 \times V_{CC}$		V
		$V_{CC}=2.3\text{V to }2.7\text{V}$	1.7		
		$V_{CC}=3\text{V to }3.6\text{V}$	2.2		
		$V_{CC}=4.5\text{V to }5.5\text{V}$	$0.7 \times V_{CC}$		
Low-level input voltage	V_{IL}	$V_{CC}=1.65\text{V to }1.95\text{V}$		$0.3 \times V_{CC}$	V
		$V_{CC}=2.3\text{V to }2.7\text{V}$		0.7	
		$V_{CC}=3\text{V to }3.6\text{V}$		0.8	
		$V_{CC}=4.5\text{V to }5.5\text{V}$		$0.25 \times V_{CC}$	
Input voltage	V_I		0	5.5	V
Output voltage	V_O		0	V_{CC}	V
Input transition rise or fall	t_r, t_f	$V_{CC}=1.8\text{V} \pm 0.15\text{V}, 2.5\text{V} \pm 0.2\text{V}$		20	ns/V
		$V_{CC}=3.3\text{V} \pm 0.3\text{V}$		10	
		$V_{CC}=5\text{V} \pm 0.5\text{V}$		5	
Operating temperature	T_A		-40	125	$^{\circ}\text{C}$

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

8.2 DC Characteristics

PARAMETER		TEST CONDITIONS	V _{CC}	TEMP	MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
V _{OH}		I _{OH} = -100μA	1.65V to 5.5V	Full	V _{CC} -0.1			V
		I _{OH} = -4mA	1.65V		1.2			
		I _{OH} = -8mA	2.3V		1.9			
		I _{OH} = -16mA	3V		2.4			
		I _{OH} = -24mA			2.3			
		I _{OH} = -32mA	4.5V		3.8			
V _{OL}		I _{OL} = 100μA	1.65V to 5.5V	Full			0.1	V
		I _{OL} = 4mA	1.65V				0.45	
		I _{OL} = 8mA	2.3V				0.3	
		I _{OL} = 16mA	3V				0.4	
		I _{OL} = 24mA					0.55	
		I _{OL} = 32mA	4.5V				0.55	
I _I	A or B inputs	V _I =5.5V or GND	0V to 5.5V	+25°C		±0.1	±1	μA
				Full			±5	
I _{off}		V _I or V _O =5.5V	0V	+25°C		±0.1	±1	μA
				Full			±10	
I _{CC}		V _I =5.5V or GND, I _O =0	1.65V to 5.5V	+25°C		0.1	1	μA
				Full			10	
ΔI _{CC}		One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND	3V to 5.5V	Full			500	μA

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

8.3 Switching Characteristics

over operating free-air temperature range; typical values are at T_A = +25°C, (unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
Propagation Delay	t _{pd}	V _{CC} =1.8V±0.15V	C _L =30pF, R _L =1kΩ		14.2		ns
		V _{CC} =2.5V±0.2V	C _L =30pF, R _L =500Ω		11.1		
		V _{CC} =3.3V±0.3V	C _L =50pF, R _L =500Ω		6.7		
		V _{CC} =5V±0.5 V	C _L =50pF, R _L =500Ω		5.3		
Input Capacitance	C _i	V _{CC} =3.3V	V _I =V _{CC} or GND		5		pF

8.4 Operating Characteristics

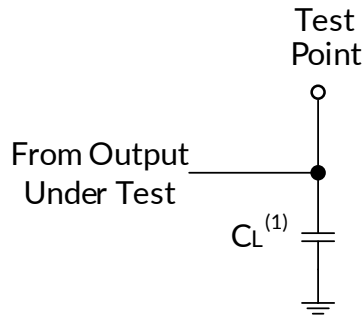
T_A=25°C

PARAMETER		TEST CONDITIONS	V _{CC} =1.65 V to 5.5 V	UNIT
			TYP	
C _{pd} ⁽¹⁾	Power dissipation capacitance	f=10MHz	28	pF

9 Parameter Measurement Information

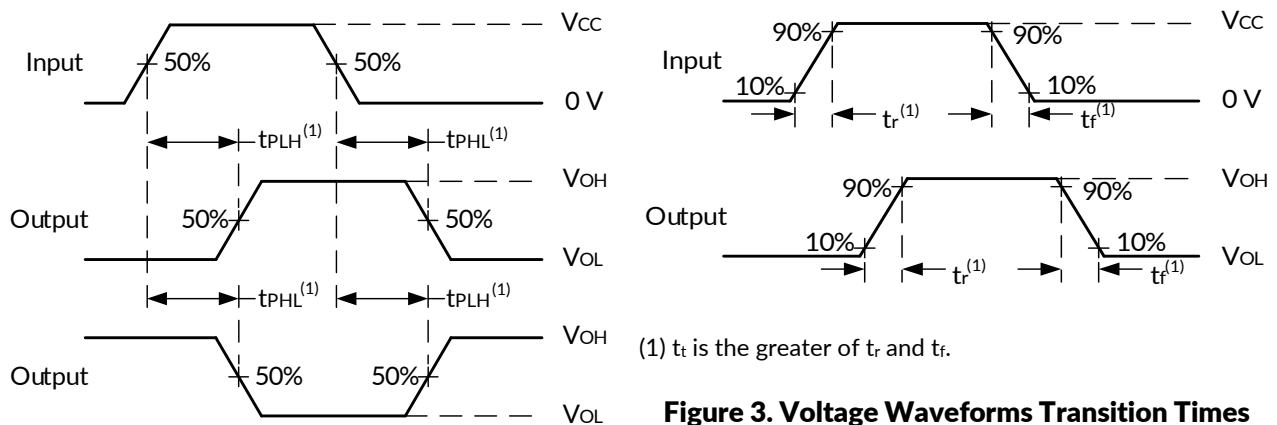
Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_t < 6 \text{ ns}$.

The outputs are measured one at a time with one input transition per measurement.



(1) $C_L = 50 \text{ pF}$ and includes probe and jig capacitance.

Figure 1. Load Circuit



(1) The maximum between t_{PLH} and t_{PHL} is used for t_{pd} .

Figure 2. Voltage Waveforms Propagation Delays

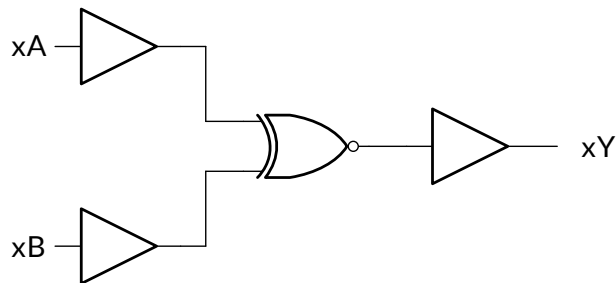
Figure 3. Voltage Waveforms Transition Times

10 Detailed Description

10.1 Overview

This device contains four independent 2-input XNOR gates. Each gate performs the Boolean function $Y = \overline{A \oplus B}$ in positive logic.

10.2 Functional Block Diagram



10.3 Device Functional Modes

Table 1. Function Table

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

11 Application and Implementation

Information in the following applications sections is not part of the Runic component specification, and Runic does not warrant its accuracy or completeness. Runic's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

In this application, a 2-input XNOR gate is used as a phase difference detector as shown in Figure 4. The remaining three gates can be used for other applications in the system, or the inputs can be grounded and the channels left unused.

The device is used to identify phase difference between a reference clock and another input clock. Whenever the clock states are different, the XNOR output will pulse HIGH until the clocks return to the same state. The output is fed into a low-pass filter to obtain a DC representation of the phase difference.

11.2 Typical Application

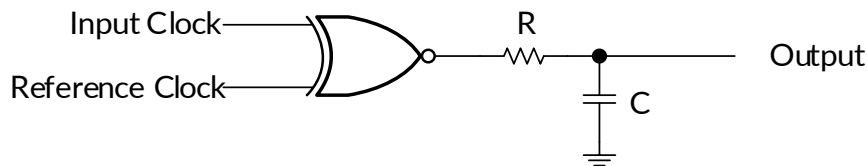


Figure 4. Typical Application Schematic

12 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the Recommended Operating Conditions. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A $0.1\mu\text{F}$ capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The $0.1\mu\text{F}$ and $1\mu\text{F}$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

13 Layout

13.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

13.2 Layout Example

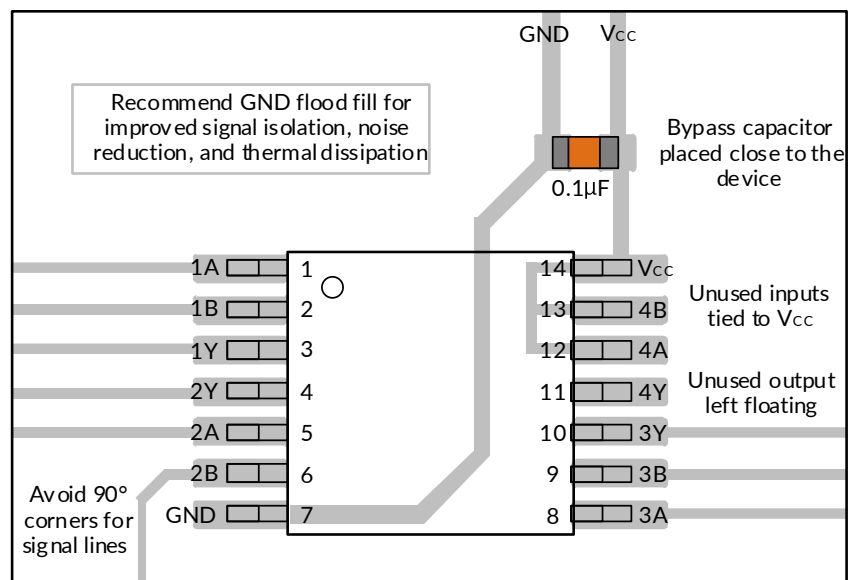
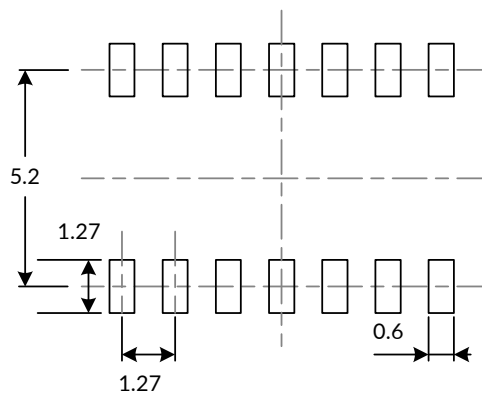
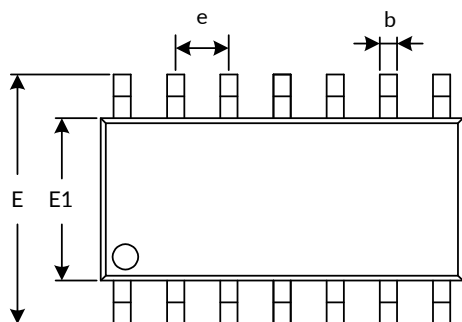


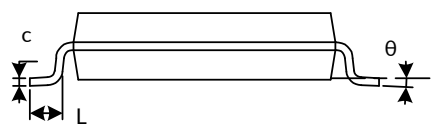
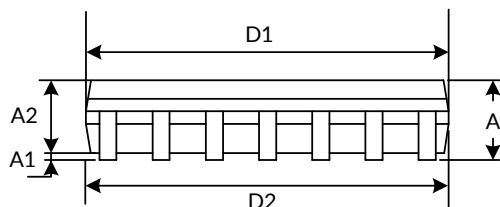
Figure 5. Layout Diagram

14 PACKAGE OUTLINE DIMENSIONS

SOP14⁽³⁾



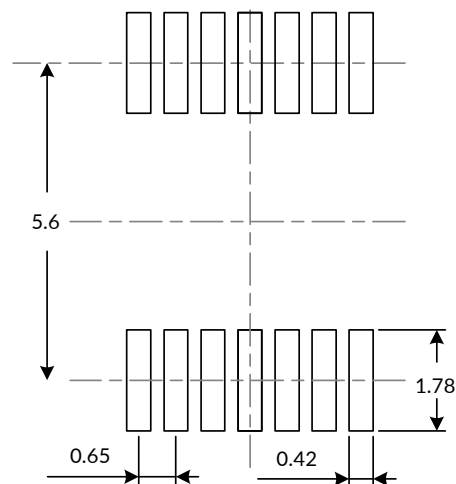
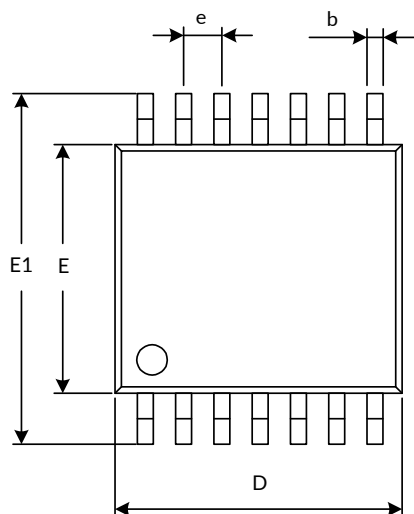
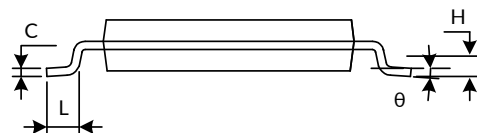
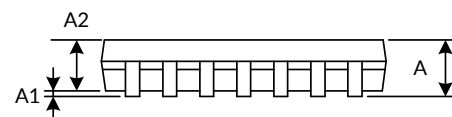
RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A ⁽¹⁾	1.500	1.700	0.059	0.067
A1	0.100	0.200	0.004	0.008
A2	1.400	1.500	0.055	0.059
b	0.375	0.425	0.015	0.017
c	0.200	0.240	0.008	0.009
D1 ⁽¹⁾	8.550	8.650	0.336	0.341
D2	8.600	8.700	0.338	0.343
e	1.270(BSC) ⁽²⁾		0.050(BSC) ⁽²⁾	
E	5.900	6.100	0.232	0.240
E1 ⁽¹⁾	3.800	3.900	0.150	0.154
L	0.500	0.700	0.020	0.028
θ	0°	8°	0°	8°

NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

TSSOP14⁽³⁾

RECOMMENDED LAND PATTERN (Unit: mm)


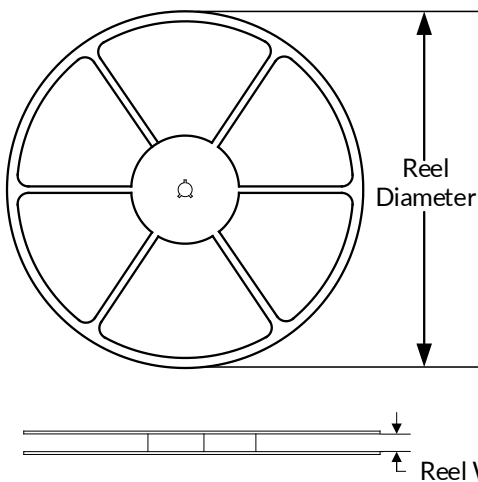
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A ⁽¹⁾		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.900	1.050	0.035	0.041
b	0.200	0.300	0.008	0.012
c	0.130	0.170	0.005	0.007
D ⁽¹⁾	4.860	5.100	0.191	0.201
E ⁽¹⁾	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.244	0.260
e	0.650(BSC) ⁽²⁾		0.026(BSC) ⁽²⁾	
L	0.450	0.750	0.018	0.030
H	0.250(TYP)		0.010(TYP)	
θ	0°	8°	0°	8°

NOTE:

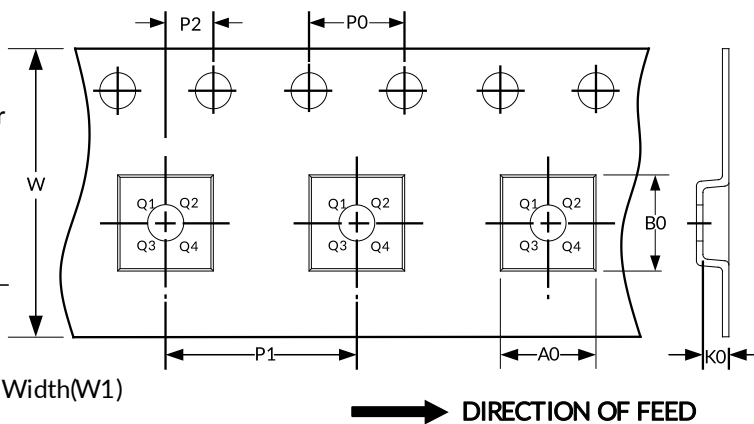
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

15 TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOP14	13"	16.4	6.60	9.30	2.10	4.0	8.0	2.0	16.0	Q1
TSSOP14	13"	12.4	6.95	5.60	1.20	4.0	8.0	2.0	12.0	Q1

NOTE:

1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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