500mA, Low Quiescent Current, Low-Noise, High PSRR, Low-Dropout Linear Regulator

1 FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified with the Grade 1**
- **Input voltage range: 2.7V to 6.5V**
- **Output voltage range:**
  - Fixed option: 1.2V to 3.3V
  - Adjustable option: 1.2V to 6V
- **Up to 500mA load current**
- **Very low dropout: 250mV at 500mA (V_{OUT}=3.3V)**
- **Low IQ: 45μA**
- **High PSRR: 75dB at 100Hz**
- **Excellent Load and Line Transient Response**
- **Stable with a Ceramic, 2.2μF, Low-ESR Output Capacitor**
- **Fast Start-Up Time: 45μs**
- **High Output Accuracy: ±0.75%**
- **Micro SIZE PACKAGES: SOT23-5, DFN2X2-6, DFN3X3-8**

2 APPLICATIONS

- **Post DC-DC Converter Ripple Filtering**
- **IP Network Cameras**
- **Macro Base Stations**
- **Thermostats**

3 DESCRIPTIONS

The RS3215-Q1 family of low-dropout (LDO), low power linear regulators offers excellent ac performance with very low ground current. High power-supply rejection ratio (PSRR), low noise, fast start-up, and excellent line and load transient responses are provided while consuming a very low 45μA (typical) ground current.

The RS3215-Q1 family of devices is stable with ceramic capacitors and uses an advanced BiCMOS fabrication process to yield a typical dropout voltage of 250mV at 500mA output. The RS3215-Q1 family of devices uses a precision voltage reference and feedback loop to achieve high accuracy of ±0.75%.

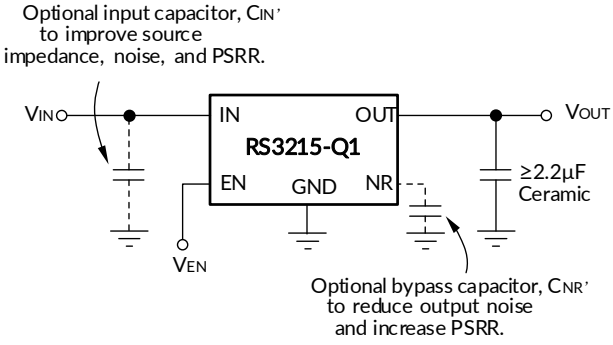
The RS3215-Q1 series is available in Green SOT23-5, DFN2X2-6 and DFN3X3-8 packages. It operates over an ambient temperature range of -40°C to 125°C.

Device Information (1)

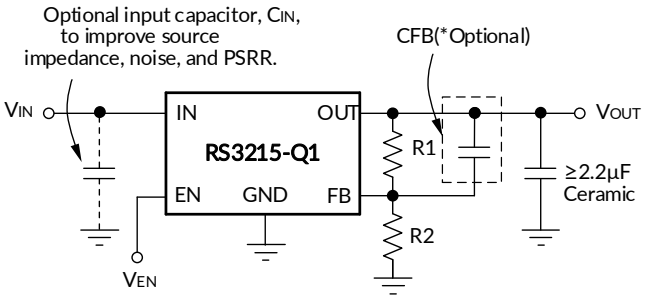
PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS3215-Q1	SOT23-5	1.60mm×2.92mm
	DFN2X2-6	2.00mm×2.00mm
	DFN3X3-8	3.00mm×3.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application

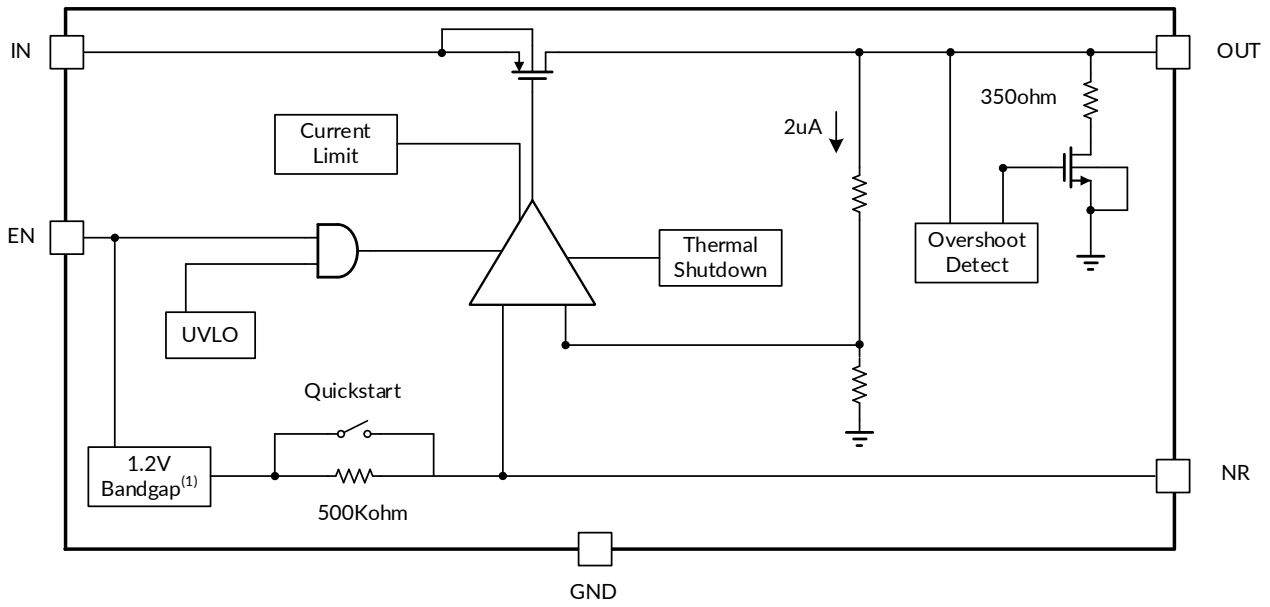


Typical Application: Fixed Voltage Version



Typical Application: Adjustable Voltage Version

4 FUNCTIONAL BLOCK DIAGRAM



(1) The 1.2V fixed voltage version has a 1V bandgap instead of a 1.2V circuit.
BG Output Voltage =1.2V & 1V

Figure 1. Fixed Voltage Versions

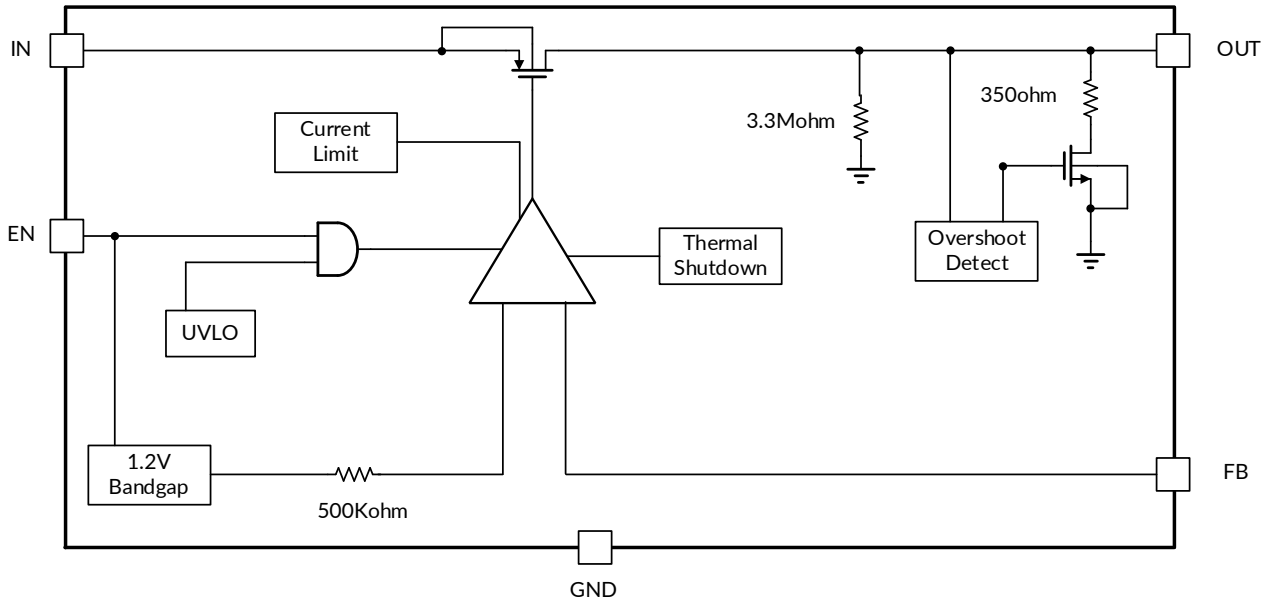


Figure 2. Adjustable Voltage Versions

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5 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2024/06/06	Preliminary version completed
A.1	2024/11/21	Initial version completed

6 PACKAGE/ORDERING INFORMATION (1)

Orderable Device	V_{OUT}(V)	TEMPERATURE RANGE	PACKAGE LEAD	Lead finish/Ball material (2)	MSL Peak Temp (3)	PACKAGE MARKING (4)	PACKAGE OPTION
RS3215-1.2XF5 -Q1	1.2	-40°C ~125°C	SOT23-5	SN	MSL1-260°-Unlimited	LF12	Tape and Reel,3000
RS3215-1.5XF5 -Q1	1.5	-40°C ~125°C	SOT23-5	SN	MSL1-260°-Unlimited	LF15	Tape and Reel,3000
RS3215-1.8XF5 -Q1	1.8	-40°C ~125°C	SOT23-5	SN	MSL1-260°-Unlimited	LF18	Tape and Reel,3000
RS3215-2.5XF5 -Q1	2.5	-40°C ~125°C	SOT23-5	SN	MSL1-260°-Unlimited	LF25	Tape and Reel,3000
RS3215-2.7XF5 -Q1	2.7	-40°C ~125°C	SOT23-5	SN	MSL1-260°-Unlimited	LF27	Tape and Reel,3000
RS3215-2.8XF5 -Q1	2.8	-40°C ~125°C	SOT23-5	SN	MSL1-260°-Unlimited	LF28	Tape and Reel,3000
RS3215-3.0XF5 -Q1	3.0	-40°C ~125°C	SOT23-5	SN	MSL1-260°-Unlimited	LF30	Tape and Reel,3000
RS3215-3.3XF5 -Q1	3.3	-40°C ~125°C	SOT23-5	SN	MSL1-260°-Unlimited	LF33	Tape and Reel,3000
RS3215-ADJ8XF5 -Q1	ADJ	-40°C ~125°C	SOT23-5	SN	MSL1-260°-Unlimited	LFAD8	Tape and Reel,3000
RS3215-1.2XTDC8-Q1	1.2	-40°C ~125°C	DFN3X3-8	NIPDAUAG /Plating Sn	MSL1-260°-Unlimited	RS3215A	Tape and Reel,5000
RS3215-1.5XTDC8-Q1	1.5	-40°C ~125°C	DFN3X3-8	NIPDAUAG /Plating Sn	MSL1-260°-Unlimited	RS3215B	Tape and Reel,5000
RS3215-1.8XTDC8-Q1	1.8	-40°C ~125°C	DFN3X3-8	NIPDAUAG /Plating Sn	MSL1-260°-Unlimited	RS3215C	Tape and Reel,5000
RS3215-2.5XTDC8-Q1	2.5	-40°C ~125°C	DFN3X3-8	NIPDAUAG /Plating Sn	MSL1-260°-Unlimited	RS3215D	Tape and Reel,5000
RS3215-2.7XTDC8-Q1	2.7	-40°C ~125°C	DFN3X3-8	NIPDAUAG /Plating Sn	MSL1-260°-Unlimited	RS3215E	Tape and Reel,5000
RS3215-2.8XTDC8-Q1	2.8	-40°C ~125°C	DFN3X3-8	NIPDAUAG /Plating Sn	MSL1-260°-Unlimited	RS3215F	Tape and Reel,5000
RS3215-3.0XTDC8-Q1	3.0	-40°C ~125°C	DFN3X3-8	NIPDAUAG /Plating Sn	MSL1-260°-Unlimited	RS3215G	Tape and Reel,5000
RS3215-3.3XTDC8-Q1	3.3	-40°C ~125°C	DFN3X3-8	NIPDAUAG /Plating Sn	MSL1-260°-Unlimited	RS3215H	Tape and Reel,5000
RS3215-ADJ8XTDC8-Q1	ADJ	-40°C ~125°C	DFN3X3-8	NIPDAUAG /Plating Sn	MSL1-260°-Unlimited	RS3215K	Tape and Reel,5000
RS3215-1.2XTDE6-Q1	1.2	-40°C ~125°C	DFN2X2-6	NIPDAUAG /Plating Sn	MSL1-260°-Unlimited	LF12	Tape and Reel,3000
RS3215-1.5XTDE6-Q1	1.5	-40°C ~125°C	DFN2X2-6	NIPDAUAG /Plating Sn	MSL1-260°-Unlimited	LF15	Tape and Reel,3000
RS3215-1.8XTDE6-Q1	1.8	-40°C ~125°C	DFN2X2-6	NIPDAUAG /Plating Sn	MSL1-260°-Unlimited	LF18	Tape and Reel,3000
RS3215-2.5XTDE6-Q1	2.5	-40°C ~125°C	DFN2X2-6	NIPDAUAG /Plating Sn	MSL1-260°-Unlimited	LF25	Tape and Reel,3000
RS3215-2.7XTDE6-Q1	2.7	-40°C ~125°C	DFN2X2-6	NIPDAUAG /Plating Sn	MSL1-260°-Unlimited	LF27	Tape and Reel,3000
RS3215-2.8XTDE6-Q1	2.8	-40°C ~125°C	DFN2X2-6	NIPDAUAG /Plating Sn	MSL1-260°-Unlimited	LF28	Tape and Reel,3000

RS3215-3.0XTDE6-Q1	3.0	-40°C ~125°C	DFN2X2-6	NIPDAUAG/Plating Sn	MSL1-260°-Unlimited	LF30	Tape and Reel,3000
RS3215-3.3XTDE6-Q1	3.3	-40°C ~125°C	DFN2X2-6	NIPDAUAG/Plating Sn	MSL1-260°-Unlimited	LF33	Tape and Reel,3000
RS3215-ADJ8XTDE6-Q1	ADJ	-40°C ~125°C	DFN2X2-6	NIPDAUAG/Plating Sn	MSL1-260°-Unlimited	LFAD8	Tape and Reel,3000

NOTE:

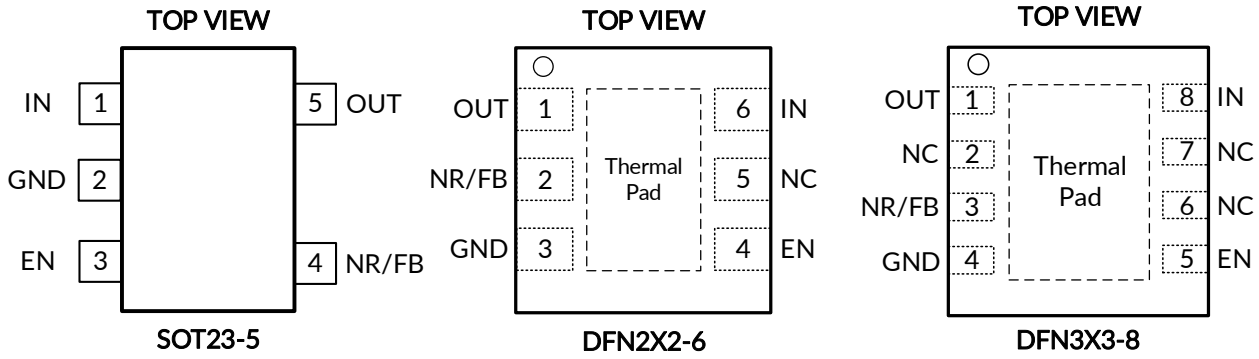
(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) Lead finish/Ball material. Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F, Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

(4) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

7 PIN CONFIGURATION AND FUNCTIONS (TOP VIEW)



Pin Description

NAME	PIN			I/O (1)	DESCRIPTION
	SOT23-5	DFN2X2-6	DFN3X3-8		
IN	1	6	8	I	Input supply.
GND	2	3	4	G	Ground.
EN	3	4	5	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. The EN pin can be connected to the IN pin if not used.
NR/FB	4	2	3	-	The NR pin is only available for the fixed voltage versions. Connecting an external capacitor to this pin bypasses noise generated by the internal band gap and allows the output noise to be reduced to very low levels. The maximum recommended capacitor is 0.01μF. The FB pin is only available for the adjustable voltage versions. This pin is the input to the control-loop error amplifier, and is used to set the output voltage of the device.
OUT	5	1	1	O	This pin is the output of the regulator. A small 2.2μF ceramic capacitor is required from this pin to ground to assure stability.
NC	-	5	2,6,7	-	Not internally connected.
-	-	Thermal Pad	Thermal Pad	-	The pad must be tied to the GND pin.

(1) I=input, O=output, G= Ground.

8 SPECIFICATIONS

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

			MIN	MAX	UNIT
V_{IN}	Input voltage		-0.3	7	V
V_{EN}	Enable input voltage		-0.3	V_{IN} + 0.3	V
V_{FB}	Input voltage		-0.3	1.6	V
V_{OUT}	Output voltage		-0.3	V_{IN} + 0.3	V
I_{OUT}	Current		Internally limited		A
θ_{JA}	Package thermal impedance (3)	SOT23-5		200	°C/W
		DFN3X3-8		60	
		DFN2X2-6		82	
T_J	Junction temperature (4)		-40	150	°C
T_{stg}	Storage temperature		-55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to the GND pin.

(3) The package thermal impedance is calculated in accordance with JESD-51.

(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

8.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-Device Model (CDM), per AEC Q100-011	±1000	
		Latch-Up (LU), per AEC Q100-004	±200	mA

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{IN}	Input supply voltage	2.7	6.5	V
V_{OUT}	Output voltage	V_{FB}	6	V
I_{OUT}	Output current	0	500	mA
T_A	Operating free-air temperature	-40	125	°C

(1) When operating at T_J near 125°C, $I_{OUT(min)}$ is 500μA.

8.4 Electrical Characteristics

Over operating temperature range (−40°C ≤ T_J ≤ 125°C), V_{IN} = V_{OUTnom} + 0.5 V or 2.7 V (whichever is greater), I_{OUT}=1mA, V_{EN} = V_{IN}, C_{OUT} = 2.2µF, and C_{NR} = 0.01µF, unless otherwise noted. For the adjustable version, V_{OUT} = 3.3V. Typical values are at T_A = 25°C.

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY AND CURRENTS							
Input Voltage (1)	V_{IN}			2.7		6.5	V
Under Voltage Lockout	UVLO	V_{IN} rising, T_J = -40°C ~125°C		2.25	2.45	2.65	V
Hysteresis	V_{HYS}	V_{IN} falling			60		mV
Quiescent Current	I_Q	I_{OUT} = 0mA, T_J = 25°C			45	70	µA
		I_{OUT} = 0mA, T_J = -40°C ~125°C				80	
Ground Pin Current	I_{GND}	10mA ≤ I_{OUT} ≤ 500mA, T_J = 25°C			70	120	µA
		10mA ≤ I_{OUT} ≤ 500mA, T_J = -40°C ~125°C				350	
Shutdown Current	I_{SD}	V_{EN} = 0V, T_J = 25°C			0.1	1	µA
		V_{EN} = 0V, T_J = -40°C ~125°C				15	
OUTPUT VOLTAGE							
Output Voltage Range	V_{OUT}	Adjustable Only		V_{FB}		6	V
Feedback Voltage	V_{FB}	Adjustable Only		1.191	1.200	1.209	V
Feedback Pin Current	I_{FB}	Adjustable Only			0.01	0.1	uA
DC Output Accuracy (1)	ΔV_{OUT}	T_J = 25°C		-0.75		0.75	%
		T_J = -40°C ~125°C		-1.5		1.5	%
Line Regulation (1)	$\Delta V_{OUT(\Delta VIN)}$	V_{OUTnom} + 0.5V ≤ V_{IN} ≤ 6.5V			0.02	0.06	%/V
Load Regulation	$\Delta V_{OUT(\Delta IOUT)}$	500µA ≤ I_{OUT} ≤ 500mA			0.002	0.006	%/mA
DROPOUT VOLTAGE							
Dropout Voltage (2)	V_{DO}	I_{OUT} = 500mA	V_{OUT}=3.3V, T_J = 25°C		250	300	mV
			V_{OUT}=3.3V, T_J = -40°C ~125°C			400	
			V_{OUT}=5.0V (Adjustable only)		195		
			V_{OUT}=6.0V (Adjustable only)		180		
POWER SUPPLY REJECTION RATIO AND NOISE							
Power Supply Rejection Ratio (3)	PSRR	V_{IN} = 3.8V, V_{OUT} = 3.3V, C_{NR} = 0.01µF, I_{OUT} = 100mA	f = 100Hz		75		dB
			f = 1kHz		64		dB
			f = 10kHz		43		dB
			f = 100kHz		23		dB
Output Noise Voltage (3)	V_N	BW = 10 Hz to 100 kHz, V_{OUT} = 3.3 V	C_{NR}=0.01µF		11×V_{OUT}		μV_{RMS}
			C_{NR}=none		45×V_{OUT}		μV_{RMS}
ENABLE AND STARTUP TIME							
Enable High(enabled)	V_{IH}	EN rising, T_J = -40°C ~125°C		1.2			V
Enable Low(shutdown)	V_{IL}	EN falling, T_J = -40°C ~125°C				0.4	V
Enable Pin Current, Enabled	I_{EN}	V_{EN} = V_{IN} = 6.5V, T_J = 25°C			0.1	1.5	µA
		V_{EN} = V_{IN} = 6.5V, T_J = -40°C ~125°C				2	

Startup Time (3)	t_{STR}	C_{NR} = none		45		μs
		C_{NR} = 0.001μF		45		μs
		C_{NR} = 0.01μF		50		μs
		C_{NR} = 0.047μF		50		μs
PROTECTIONS						
Output Current Limit	I_{LIM}	V_{OUT} = 0.9 × V_{OUTnom}, V_{IN} = V_{OUTnom} + 0.5V, V_{IN} ≥ 2.7V	500	1150	1600	mA
Thermal Shutdown Temperature (3)	T_{SD}	Shutdown, temperature increasing		150		°C
		Reset, temperature decreasing		135		°C

NOTES:

1. Minimum V_{IN} = V_{OUT} + V_{DO} or 2.7V, whichever is greater.
2. V_{DO} FT test method: test the V_{OUT} voltage at V_{OUTnom} +V_{DOMAX} with output current.
3. Guaranteed by design and characterization, not a FT item.

8.5 Typical Performance Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

Over operating temperature range (−40°C ≤ T_J ≤ 125°C), V_{IN} = V_{OUTnom} + 0.5V or 2.7V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, C_{OUT} = 2.2µF, and C_{NR} = 0.01µF, unless otherwise noted.

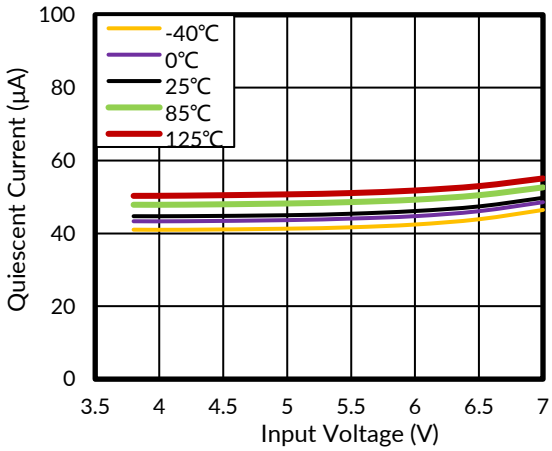


Figure 3. Quiescent Current vs Input Voltage

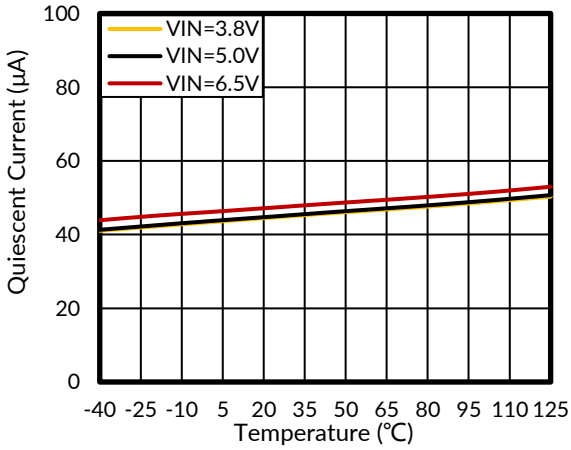


Figure 4. Quiescent Current vs Temperature

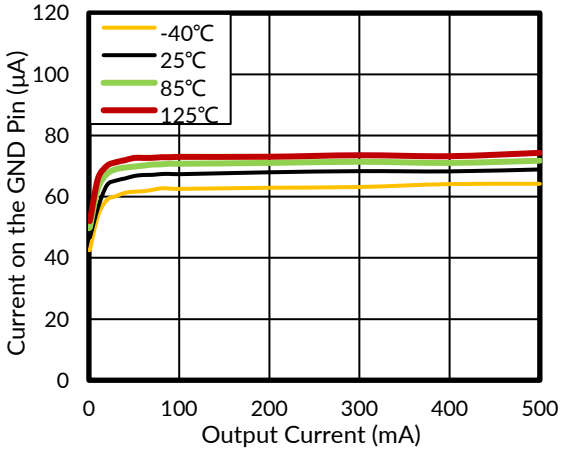


Figure 5. Ground Pin Current vs Output Current

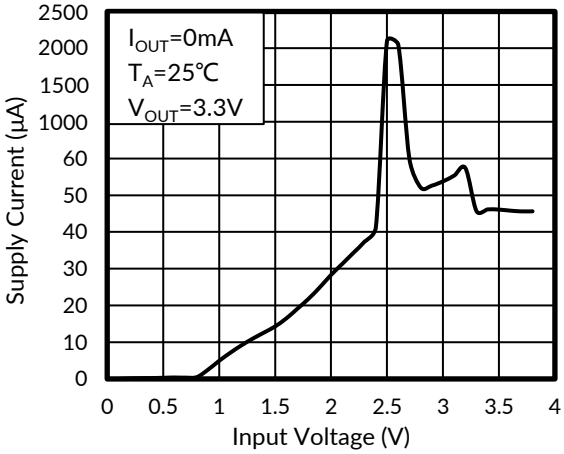


Figure 6. Supply Current vs Input Voltage

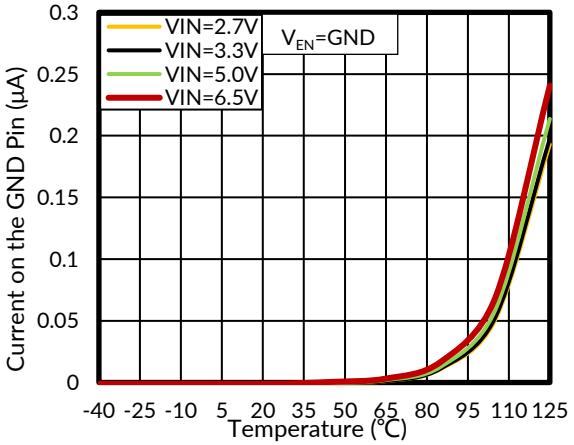


Figure 7. Shutdown Current vs Temperature

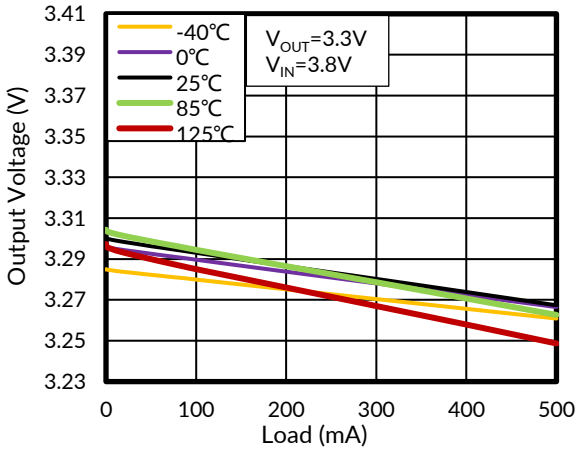


Figure 8. Load Regulation

Typical Performance Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

Over operating temperature range (−40°C ≤ T_J ≤ 125°C), V_{IN} = V_{OUTnom} + 0.5V or 2.7V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, C_{OUT} = 2.2µF, and C_{NR} = 0.01µF, unless otherwise noted.

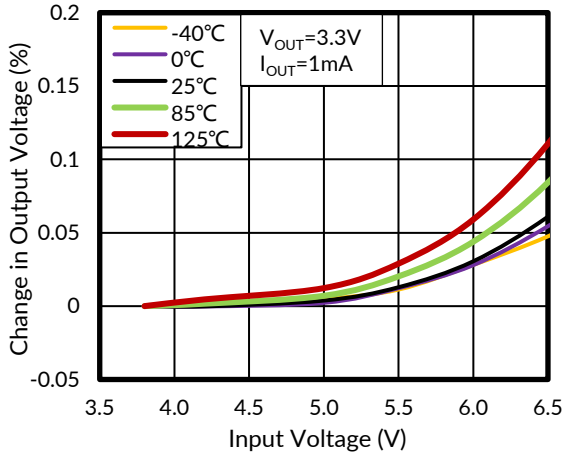


Figure 9. Line Regulation

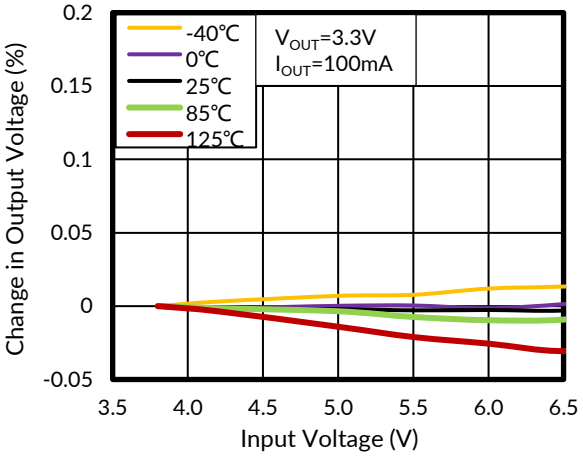


Figure 10. Line Regulation

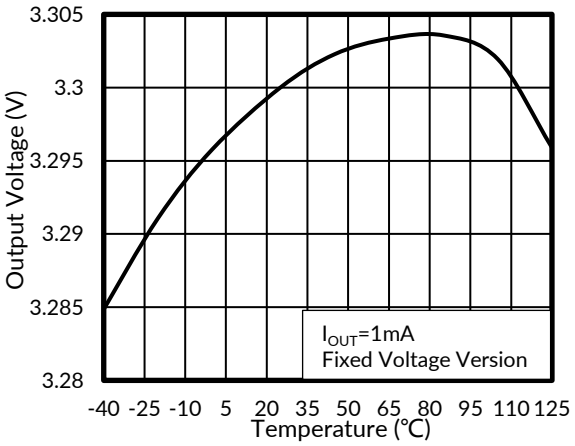


Figure 11. Output Voltage vs Junction Temperature

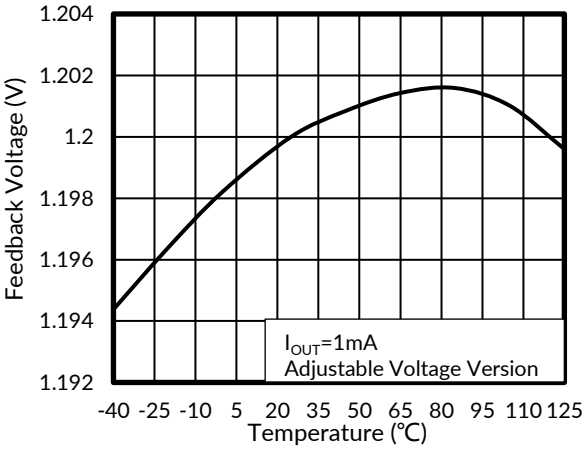


Figure 12. Feedback Voltage vs Junction Temperature

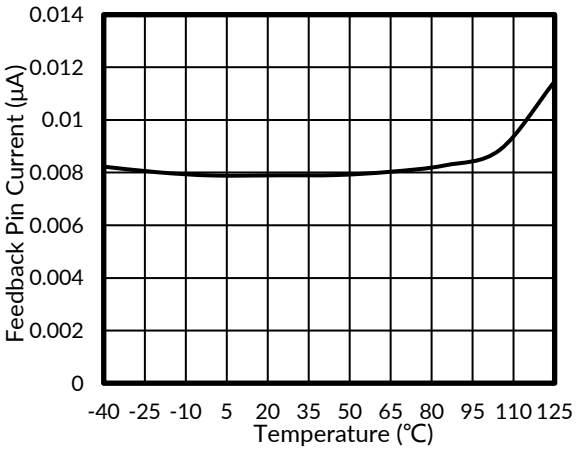


Figure 13. Feedback Pin Current vs Junction Temperature

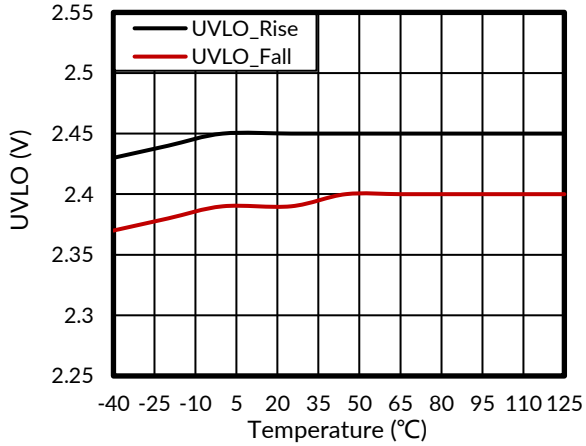


Figure 14. UVLO vs Junction Temperature

Typical Performance Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

Over operating temperature range (−40°C ≤ T_J ≤ 125°C), V_{IN} = V_{OUTnom} + 0.5V or 2.7V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, C_{OUT} = 2.2µF, and C_{NR} = 0.01µF, unless otherwise noted.

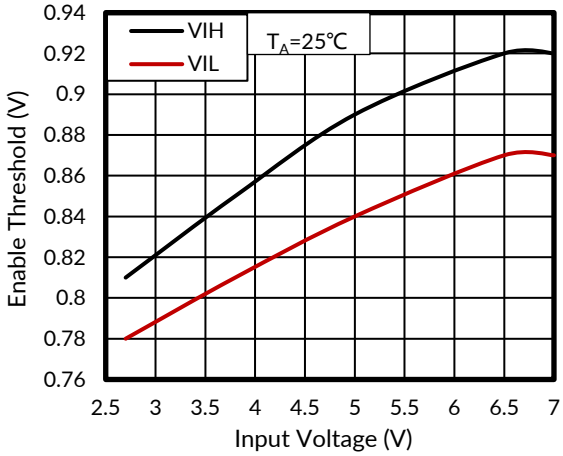


Figure 15. Enable Threshold vs Input Voltage

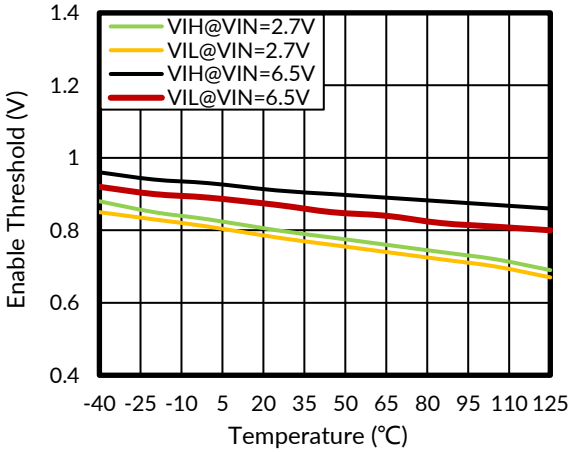


Figure 16. Enable Threshold vs Junction Temperature

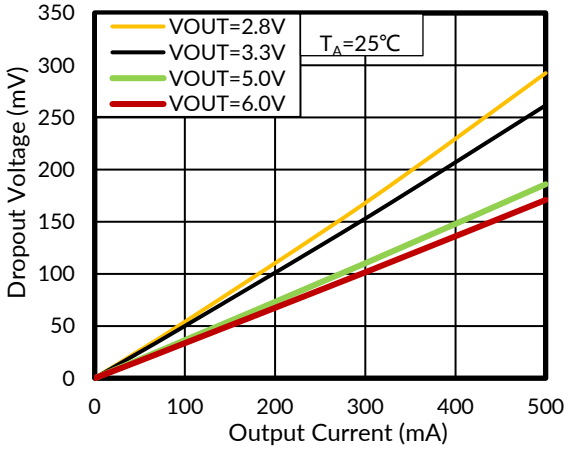


Figure 17. Dropout Voltage vs Output Current

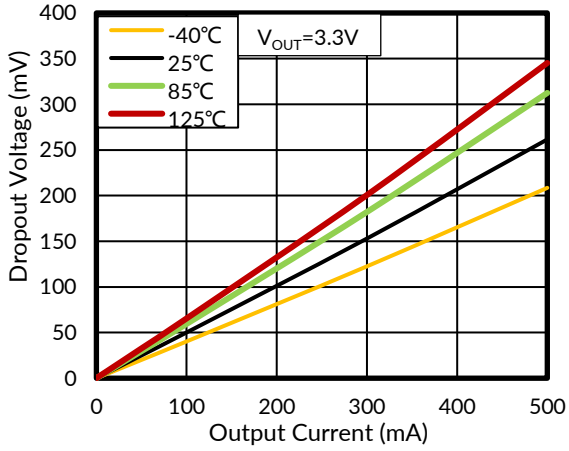


Figure 18. Dropout Voltage vs Output Current

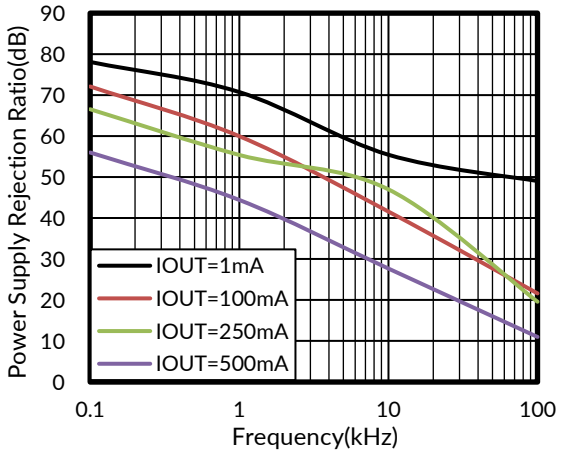


Figure 19. Power Supply Rejection Ratio vs Frequency

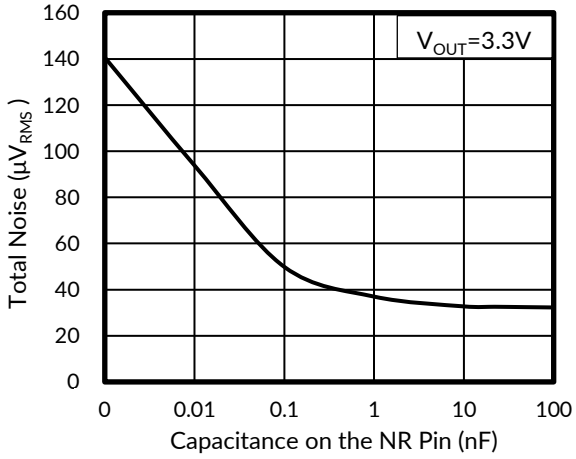


Figure 20. RMS Noise vs C_{NR}

Typical Performance Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

Over operating temperature range (−40°C ≤ T_J ≤ 125°C), V_{IN} = V_{OUTnom} + 0.5V or 2.7V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, C_{OUT} = 2.2µF, and C_{NR} = 0.01µF, unless otherwise noted.

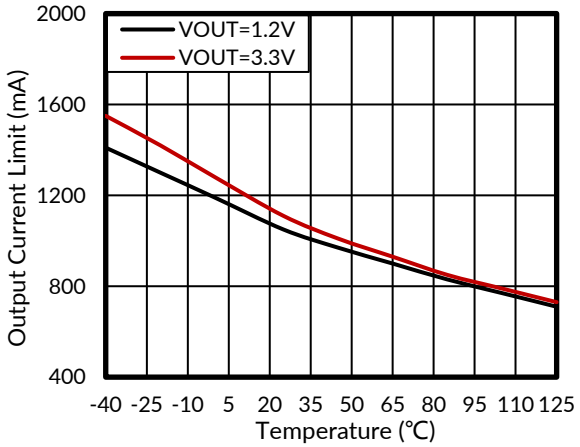


Figure 21. Output Current Limit vs Temperature

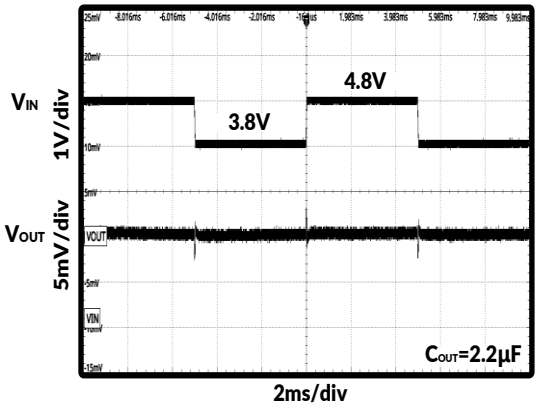


Figure 22. Line Transient Response

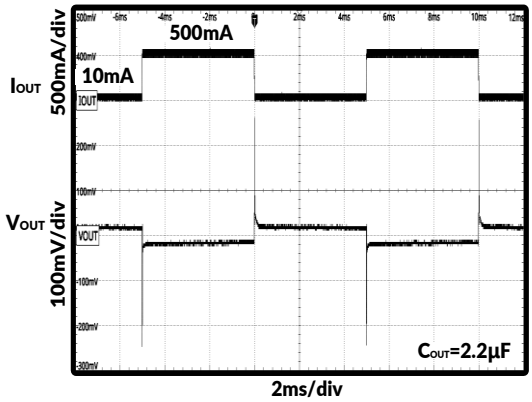


Figure 23. Load Transient Response

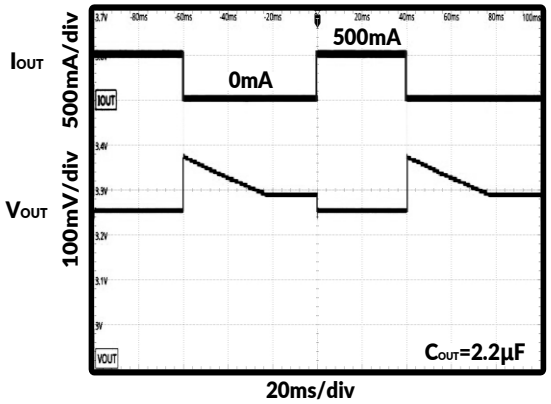


Figure 24. Load Transient Response

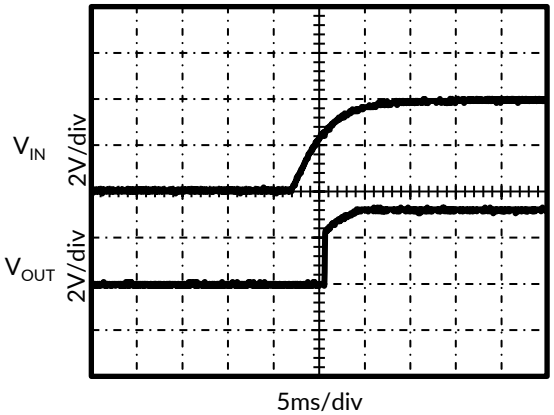


Figure 25. Power On

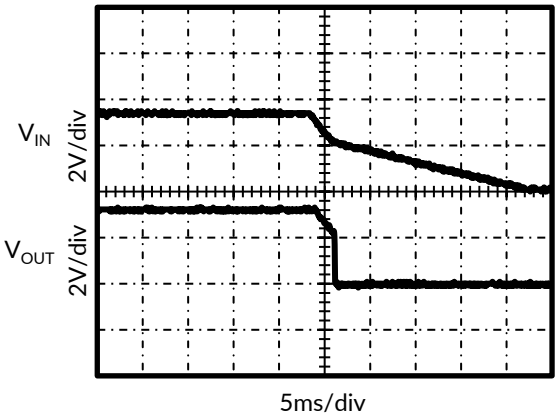


Figure 26. Power Off

Typical Performance Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

Over operating temperature range (−40°C ≤ T_J ≤ 125°C), V_{IN} = V_{OUTnom} + 0.5V or 2.7V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, C_{OUT} = 2.2µF, and C_{NR} = 0.01µF, unless otherwise noted.

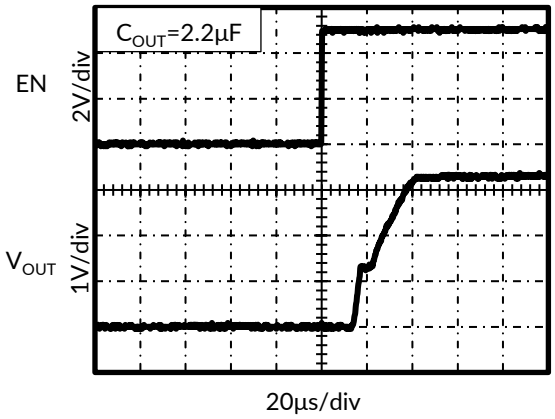


Figure 27. Turn-On Response Using EN

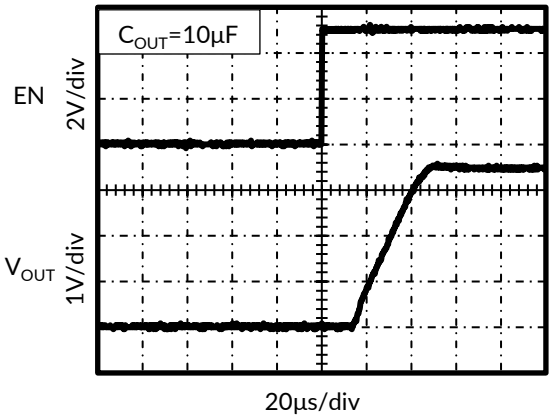


Figure 28. Turn-On Response Using EN

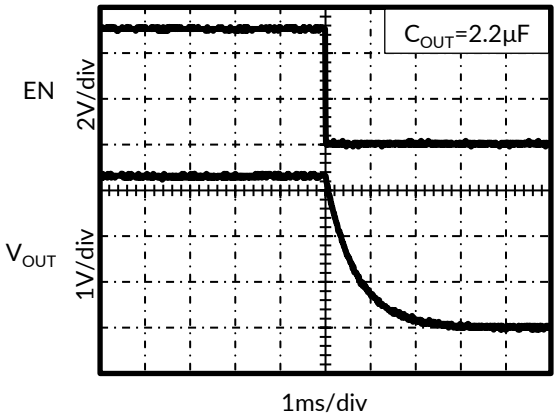


Figure 29. Turn-Off Response Using EN

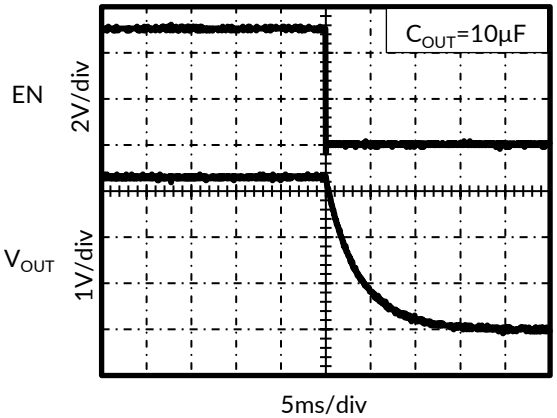


Figure 30. Turn-Off Response Using EN

9 FEATURE DESCRIPTION

9.1 Internal Current-Limit

The RS3215-Q1 internal current-limit helps protect the regulator during fault conditions. During current-limit, the output sources a fixed amount of current that is largely independent of the output voltage. For reliable operation, do not operate the device in current-limit for extended periods of time.

The RS3215-Q1 family of devices has a built-in body diode that conducts current when the voltage at the OUT pin exceeds the voltage at the IN pin. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting can be appropriate.

9.2 Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage TTL-CMOS levels. When shutdown capability is not required, the EN pin can be connected to the IN pin.

9.3 Startup and Noise Reduction Capacitor

Fixed voltage versions of the RS3215-Q1 family of devices use a quick-start circuit to fast-charge the noise reduction capacitor, C_{NR}, if present. This architecture allows the combination of very-low output noise and fast startup times. The NR pin is high impedance so a low-leakage C_{NR} capacitor must be used. Most ceramic capacitors are appropriate in this configuration. A high-quality, C0G-type (NP0) dielectric ceramic capacitor is recommended for C_{NR} when used in environments where abrupt changes in temperature can occur.

9.4 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases the transient response duration. In the adjustable version, adding C_{FB} between the OUT and FB pins improves stability and transient response performance. The transient response of the RS3215-Q1 family of devices is enhanced by an active pulldown that engages when the output overshoots by approximately 4.5% or more when the device is enabled. When enabled, the pull-down device behaves like a 350Ω resistor to ground.

9.5 Undervoltage Lockout (UVLO)

The RS3215-Q1 family of devices uses an undervoltage lockout circuit to keep the output shut off until the internal circuitry is operating properly.

9.6 Disabled

The device is disabled under the following conditions:

- The input voltage is less than the UVLO threshold minus V_{HYS}, or has not yet exceeded the UVLO threshold.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold. When disenabled, the pull-down device behaves like a 350Ω resistor to ground.
- The device junction temperature is greater than the thermal shutdown temperature.

10 TYPICAL APPLICATION

10.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, connecting a 0.1μF to 1μF low-equivalent series resistance (ESR) capacitor across the input supply near the regulator is good analog design practice. This capacitor counteracts reactive input sources and improves transient response and ripple rejection. A higher value capacitor can be necessary if large, fast, rise-time load transients are anticipated or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1μF input capacitor can be necessary to ensure stability.

The RS3215-Q1 family of devices is designed to be stable with standard ceramic output capacitors of values 2.2μF or larger. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature.

10.2 Adjustable Device Feedback Resistors

The adjustable-version device requires external feedback divider resistors to set the output voltage. V_{OUT} is set using the feedback divider resistors, R_1 and R_2, according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (1)$$

To ignore the FB pin current error term in the V_{OUT} equation, set the feedback divider current to 100x the FB pin current listed in the Electrical Characteristics table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq V_{OUT} / (I_{FB} \times 100) \quad (2)$$

10.3 Feed-Forward Capacitor(*Optional)

For the adjustable-voltage version device, a feed-forward capacitor (CFB) can be connected from the OUT pin to the FB pin. CFB improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended CFB values are listed in the table1.

Table1

VOUT (V)	COUT (μF)	R2 (kΩ)	CFB (pF)
1.8	2.2 or 4.7 or 10 or 22	220	22
		100	47
		47	100
3.3	2.2 or 4.7 or 10 or 22	220	22
		100	47
		47	100
5.0	2.2 or 4.7 or 10 or 22	220	22
		100	47
		47	100

11 POWER SUPPLY RECOMMENDATIONS

The device is designed to operate from an input voltage supply range between 2.7V and 6.5V. The input voltage range must provide adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve output noise.

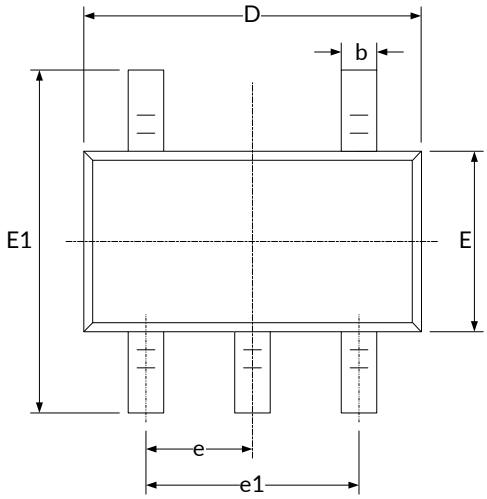
12 LAYOUT

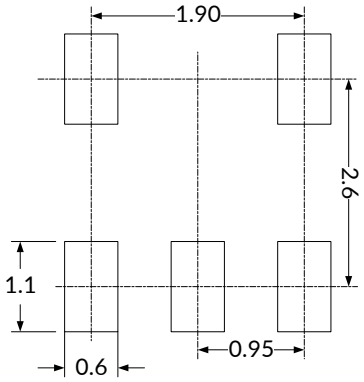
For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO component connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the printed circuit board (PCB) itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shields the LDO from noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the exposed thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

To improve ac performance (such as PSRR, output noise, and transient response), designing the board with separate ground planes for V_{IN} and V_{OUT} is recommended, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

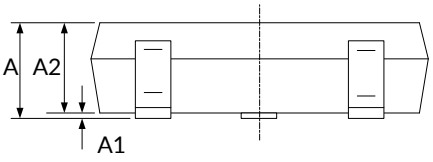
13 PACKAGE OUTLINE DIMENSIONS

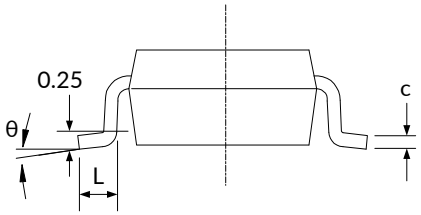
SOT23-5 (3)





RECOMMENDED LAND PATTERN (Unit: mm)



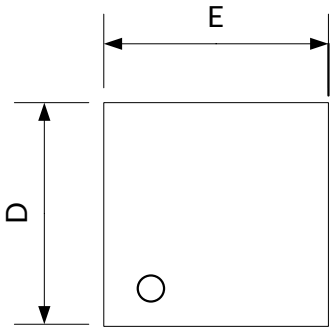


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.250		0.049
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.360	0.500	0.014	0.020
c	0.100	0.200	0.004	0.008
D (1)	2.826	3.026	0.111	0.119
E (1)	1.526	1.726	0.060	0.068
E1	2.600	3.000	0.102	0.118
e	0.950(BSC) (2)		0.037(BSC) (2)	
e1	1.800	2.000	0.071	0.079
L	0.350	0.600	0.014	0.024
θ	0°	8°	0°	8°

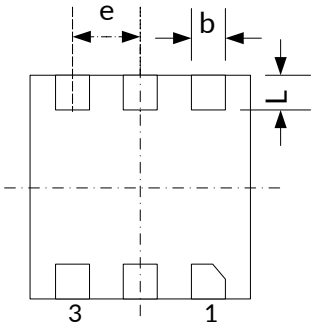
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

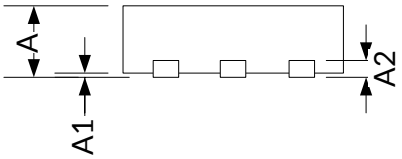
DFN2X2-6 (2)



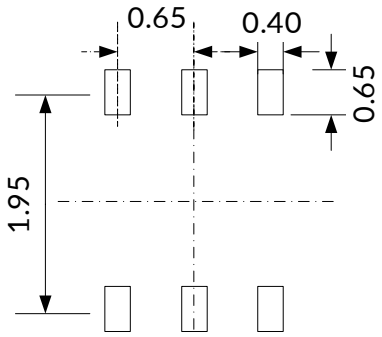
TOP VIEW



BOTTOM VIEW



SIDE VIEW



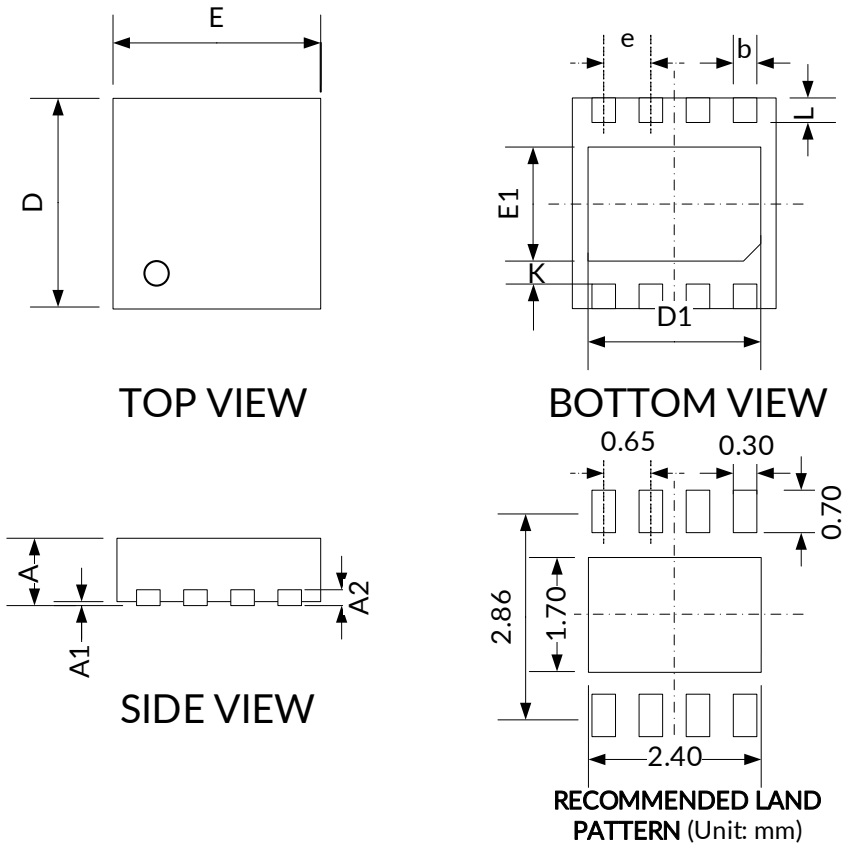
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203(TYP)		0.008(TYP)	
b	0.250	0.350	0.010	0.012
D (1)	1.900	2.100	0.075	0.083
E (1)	1.900	2.100	0.075	0.083
e	0.650(TYP)		0.026(TYP)	
L	0.250	0.400	0.010	0.018

NOTE:

1. Plastic or metal protrusions of 0.075mm maximum per side are not included.
2. This drawing is subject to change without notice.

DFN3X3-8 (3)



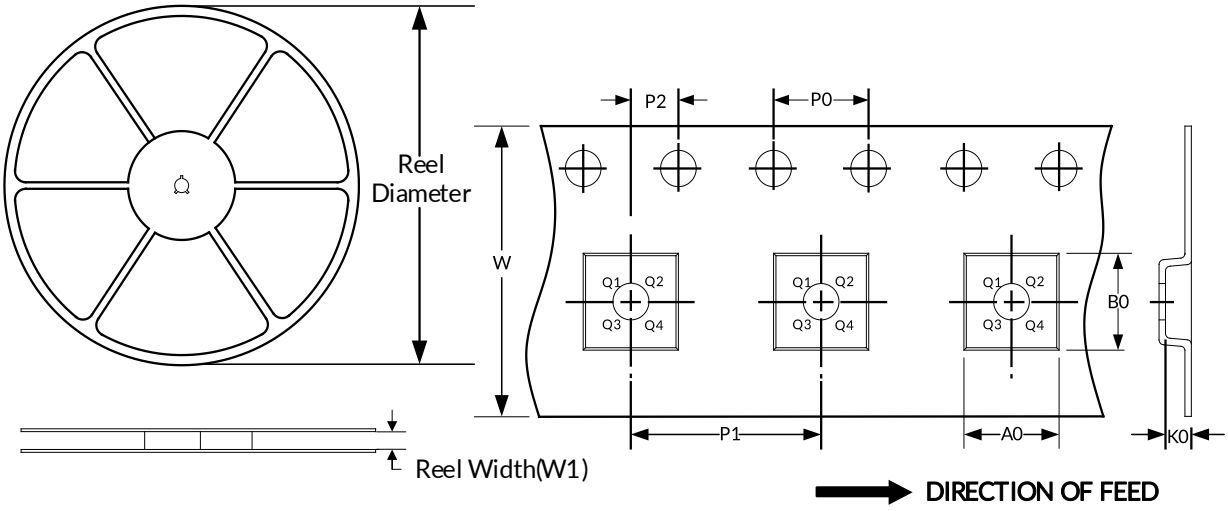
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF (2)		0.008 REF (2)	
b	0.200	0.300	0.008	0.012
D (1)	2.900	3.100	0.114	0.122
D1	2.250	2.350	0.089	0.093
E (1)	2.900	3.100	0.114	0.122
E1	1.450	1.550	0.057	0.061
e	0.650 TYP		0.026 TYP	
L	0.425	0.525	0.017	0.021
K	0.200 REF (2)		0.008 REF (2)	

NOTE:

1. Plastic or metal protrusions of 0.075mm maximum per side are not included.
2. REF is the abbreviation for Reference.
3. This drawing is subject to change without notice.

14 TAPE AND REEL INFORMATION

REEL DIMENSIONS **TAPE DIMENSION**



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT23-5	7”	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
DFN2X2-6	7”	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q1
DFN3X3-8	13”	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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