RS555 Precision Timers

1 FEATURES

- **A stable or Monostable Operation**
- **Support for Rail-To-Rail CMOS Output**
- **High Current Output Capacity**
  Sink: 100mA (Typical)
  Source: 10mA (Typical)
- **Output is Fully Compatible with CMOS, TTL and MOS**
- **Low Power Current Reduces Spiking during the Output Transient**
- **4.5V to 16 V Single Power Supply Operation**
  (The Maximum Power Output is 0.5W)
- **Functionally Changeable with other 555 Chips, has the Same Pin Arrangement**
- **Working Temperature Range: -40℃~125℃**

2 APPLICATIONS

- **Accurate Timing**
- **Pulse Generating**
- **Order Timing**
- **Time Delay Generation**
- **Pulse-Width Modulation**
- **Linear Ramp Generator**
- **Car Lights and LED Lighting**
- **Remote Message Processing**

3 DESCRIPTIONS

RS555 is a timing chip manufactured using high-voltage CMOS technology. The timer is fully compatible with the CMOS, TTL, and MOS. The operating frequency is up to 6MHz. Low power consumption can be maintained throughout the entire power supply voltage range.

The threshold and trigger levels normally are two-thirds and one-third, respectively of V_{DD}. These levels can be altered by use of the control-voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set, and the output goes high. If the trigger input is above the threshold level, the flip-flop is reset and the output is low.

The reset Input (RESET) can be used to start a new timing cycle. When the RESET is low, the output can be pulled down low. By default, the RESET pins are connected high.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE(NOM)
RS555	SOP8	4.90mm×3.90mm
	MSOP8	3.00mm×3.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

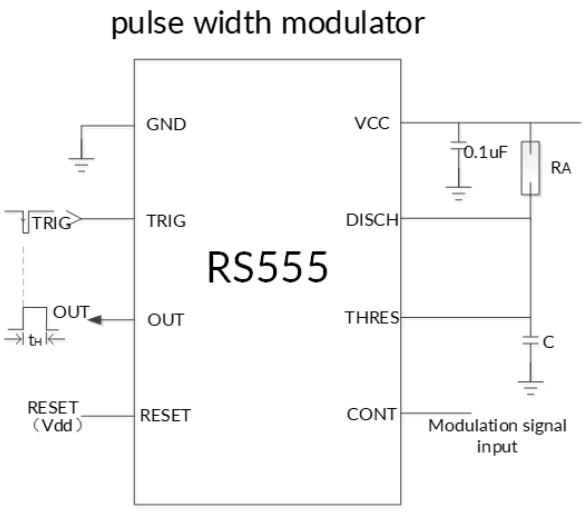

Figure 1. RS555 Typical application

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4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.1	2023/11/08	Version I
A.2	2024/03/11	Added PACKAGE/ORDERING INFORMATION and TAPE AND REEL INFORMATION
A.3	2024/05/07	Add descriptions on test waveforms
A.4	2024/05/09	Add the annotation and refine the test data
A.5	2024/09/19	Date update for V2 version
A.6	2024/12/11	Add MSOP8 Package

5 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	PACKAGE LEAD	TEMPERATURE RANGE	PACKAGE MARKING (2)	MSL (3)	PACKAGE OPTION
RS555	RS555XK	SOP8	-40℃ ~125℃	RS555	MSL3	Tape and Reel, 4000
	RS555XM	MSOP8	-40℃ ~125℃	RS555	MSL3	Tape and Reel, 4000

NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

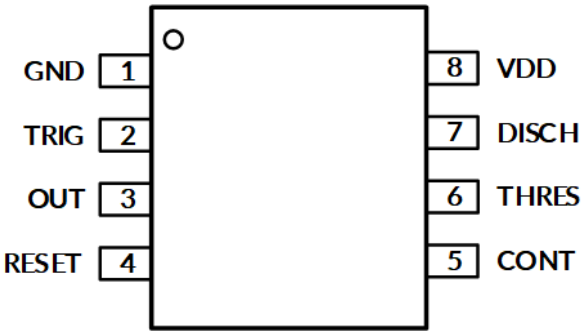
(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F, Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

6 SUMMARY

A low power consumption timing chip, support the power working range of 4.5V~16V. the maximum power is up to 0.5W. Support the sink current of 100mA and the source current of 10mA. It can be applied to timing, signal modulation, time delay and other occasions. The output frequency is up to 6MHz. the chip package is SOP8 and MSOP8.

7 PIN CONFIGURATION AND FUNCTIONS

TOP VIEW



SOP8/MSOP8

Table 1 Pin Functions

Pin Num	NAME	I/O	DESCRIPTION
5	CONT	I	Controls comparator thresholds, Outputs 2/3 $V_{DD,}$ allows bypass capacitor connection
7	DISCH	O	Open drain output to discharge timing capacitor
1	GND	P	Ground
3	OUT	O	High current timer output signal
4	RESET	I	Active low reset input forces output and discharge low
6	THRES	I	End of timing input. THRES>CONT sets output low and discharge low
2	TRIG	I	Start of timing input. TRIG<1/2 CONT sets output high and discharge open
8	VDD	P	Input supply voltage,4.5V to 16V

8 ELECTROSTATIC DISCHARGE CAUTION

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

PARAMETER			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	HBM	2000	V
		CDM	1500	
		Latch Up	400	mA

This integrated circuit can be damaged when encountering high energy ESD. Therefore, appropriate ESD prevention measures should be taken to avoid device performance degradation or loss of function.

9 TECHNICAL SPECIFICATIONS

9.1 Electrical Character

Table 2 Operating conditions

PARAMETER	MIN	TYP	MAX	UNIT
V_{DD} Supply voltage	4.5		16	V
T_A Operating free-air temperature	-40	27	125	℃

Table 3 electrical character V_{DD}=5V

Over operation free-air temperature range, V_{DD}=5V (unless otherwise noted).

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT} THRES voltage level	25℃			3.35		V
	the whole range(1)		2.7		3.9	
$V_{I(TRIG)}$ TRIG voltage level	25℃			1.65		V
	the whole range		1.26		2.1	
$V_{I(RESET)}$ RESET voltage level	25℃			1.74		V
	the whole range		0.1		2.1	
Control voltage as a percentage of the supply voltage	the whole range			65.4%		
DISCH switch on-state voltage	$I_{I(RESET)}$=10mA	25℃		0.19		V
		the whole range			0.6	
V_{OH} High-level output voltage	I_{OH}=-1mA	25℃		4.9		V
		the whole range	4.1			
V_{OL} Low-level output voltage	I_{OL}=8mA	25℃		0.21		V
		the whole range			0.6	
	I_{OL}=5mA	25℃		0.11		
		the whole range			0.4	
	I_{OL}=3.2mA	25℃		0.03		
		the whole range			0.35	
I_{DD} Supply current(2)	25℃			240		μA
	the whole range				730	

(1) The whole range: the operating temperature T_A is -40℃~125℃

(2) These values apply to normal running configurations, Where THRES is directly linked to either DISCH or TRIG

Table 4 electrical character V_{DD}=15V

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT} THRES voltage level	25°C			10.01		V
	the whole range(1)		9.3		10.7	
$V_{I(TRIG)}$ TRIG voltage level	25°C			5		V
	the whole range		4.5		5.5	
$V_{I(RESET)}$ RESET voltage level	25°C			1.74		V
	the whole range		0.1		2.1	
Control voltage as a percentage of the supply voltage	the whole range			65.2%		
DISCH switch on-state voltage	$I_{I(RESET)}$ =100mA	25°C		0.5		V
		the whole range			1.75	
V_{OH} High-level output voltage	I_{OH} =-10mA	25°C		13.8		V
		the whole range	12.6			
	I_{OH} =-5mA	25°C		14.3		V
		the whole range	13.6			
	I_{OH} =-1mA	25°C		14.8		V
		the whole range	14.25			
V_{OL} Low-level output voltage	I_{OL} =100mA	25°C		1.05		V
		the whole range			3.4	
	I_{OL} =50mA	25°C		0.51		
		the whole range			1.45	
	I_{OL} =10mA	25°C		0.1		
		the whole range			0.43	
I_{DD} Supply current(2)	25°C			300		μA
	the whole range				1000	

(1) The whole range: the operating temperature T_A is -40°C~125°C

(2) These values apply to normal running configurations, Where THRES is directly linked to either DISCH or TRIG

9.2 Operating Characteristics

Table 5 V_{DD}=5V~15V

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Initial error of timing interval(1)	V_{DD}=5V to 15V, C_T=0.1μF, R_A=R_B=1kΩ to 100kΩ	25°C		1.5	3.8	%
Supply-voltage sensitivity of timing interval(2)	V_{DD}=5V to 15V, C_T=0.1μF, R_A=R_B=1kΩ to 100kΩ	25°C		0.3	0.5	%/V
t_r Output-pulse rise time	R_L=10MΩ, C_L=10pF	25°C		18		ns
t_f Output-pulse fall time	R_L=10MΩ, C_L=10pF	25°C		9		ns
f_{max} Maximum frequency in the A steady-state mode	R_A=470Ω, C_T=200pF, R_B=200Ω	25°C		3.24		MHz

(1) The timing interval error is the difference between the measurement and the mean of the random sample in each process trial

(2) Voltage sensitivity is the ratio of the frequency change rate and the change amount of voltage

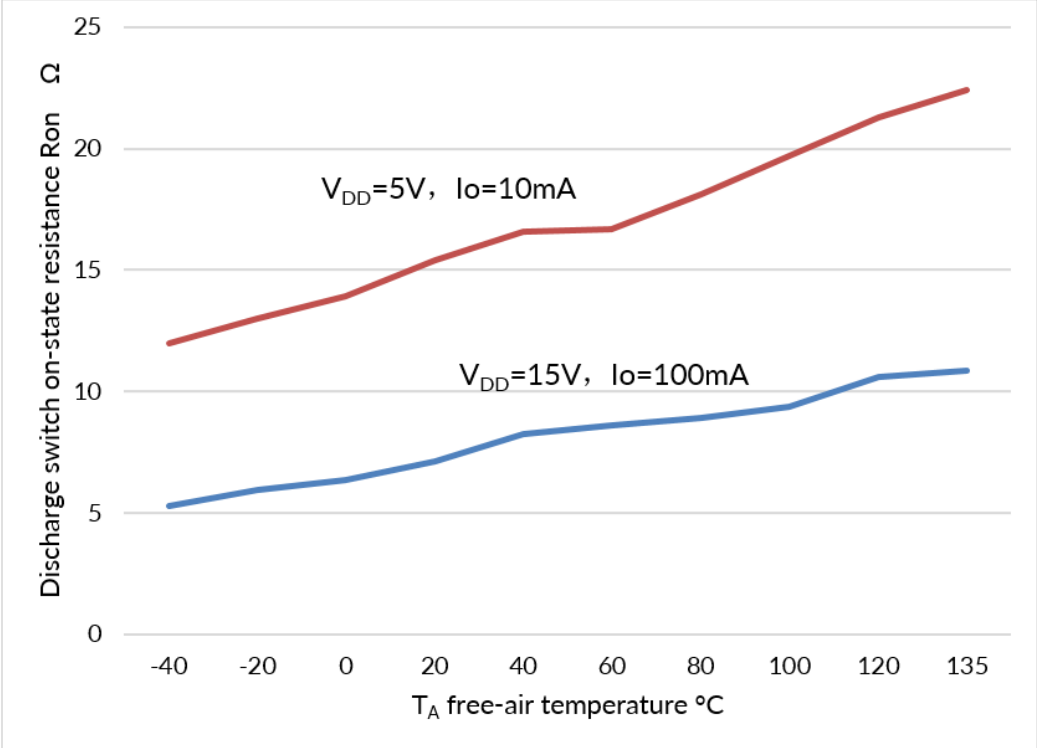


Figure 2. The relationship between the discharge-on state resistance and the temperature

10 FUNCTIONAL BLOCK DIAGRAM

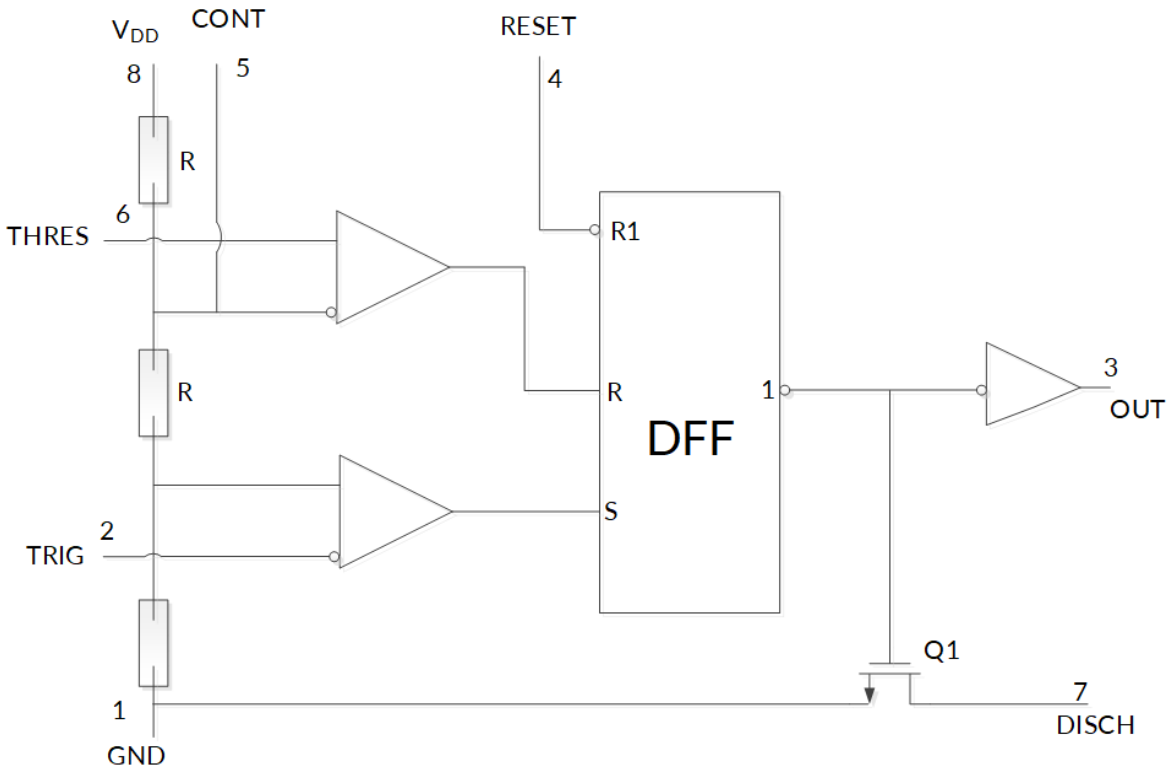


Figure 3. A Schematic diagram of the RS555 chip

11 FEATURE DESCRIPTION

11.1 Mono-stable Operation

For mono-stable operation, the test circuit may be connected as described in Figure 3. If the output is low, application of a negative-going pulse to the trigger (TRIG) sets the flip-flop. At this time, the capacitor C_T is charged through the R_A, the output changes at a high level until the voltage across the capacitor reaches the threshold voltage of the threshold (THRES) input. If TRIG has returned to a high level, the output of the threshold comparator resets the flip-flop, drives the output low, and discharges C_T through Q1.

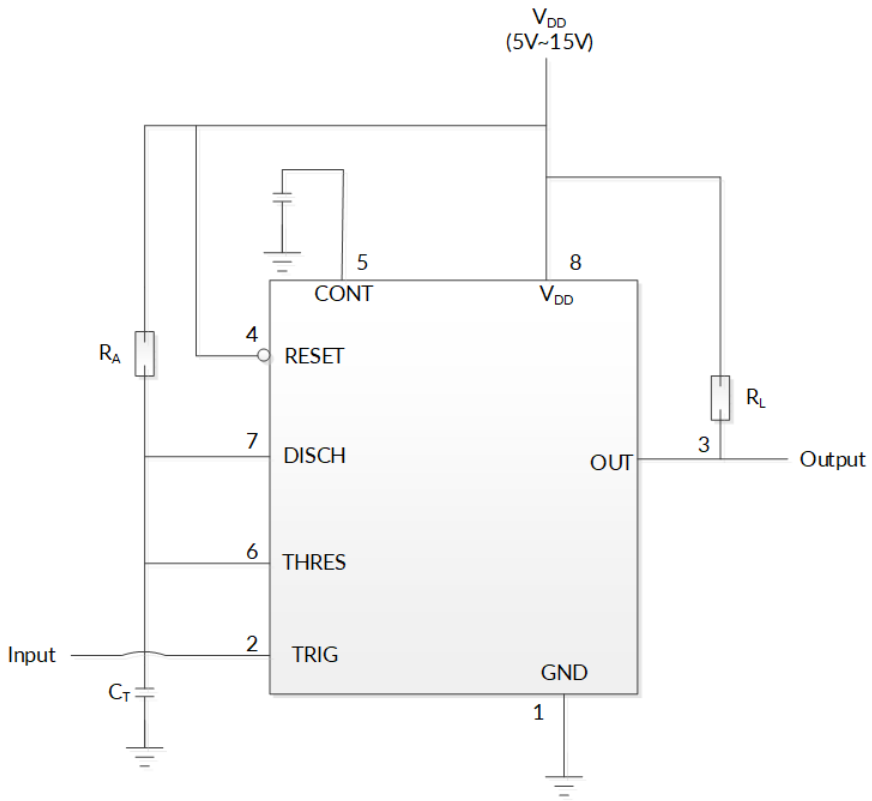


Figure 4. Circuit for Monostable Operation

Then the monostable operating state is initiated when the voltage applied to the TRIG pin drops below the trigger threshold. After entry, this sequence will only end if TRIG maintains a high level within at least 10μs before the end of the timing interval. Due to the threshold level and voltage of Q1, the output pulse duration at the OUT end is approximately $t_w = 1.1R_AC_T$. Figure 6 is the time constant plot corresponding to the different values of R_A and C_T.

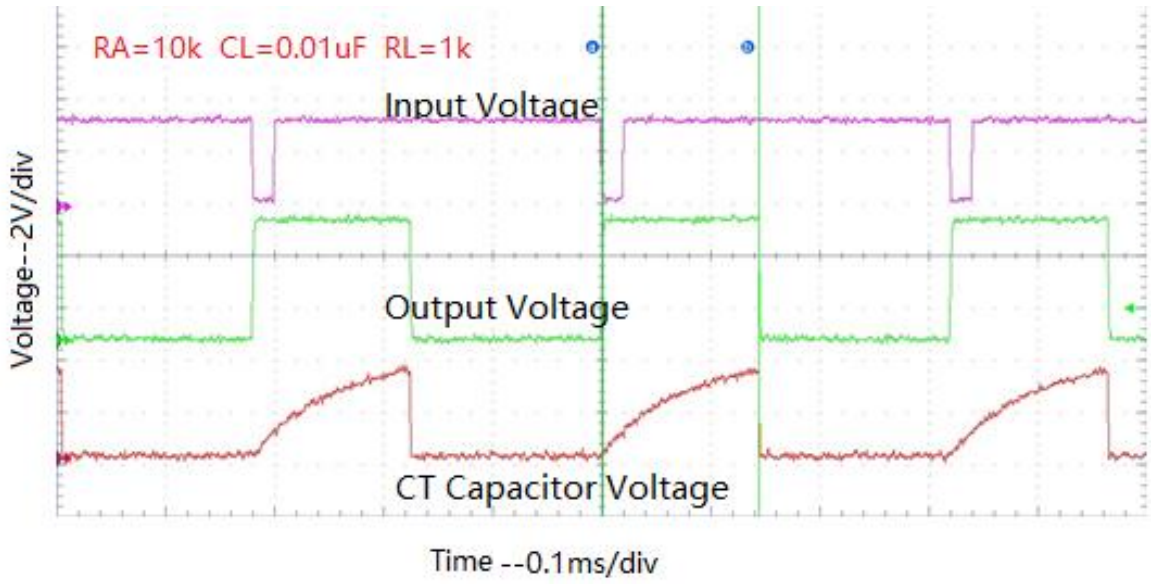


Figure 5. Typical Monostable Waveforms

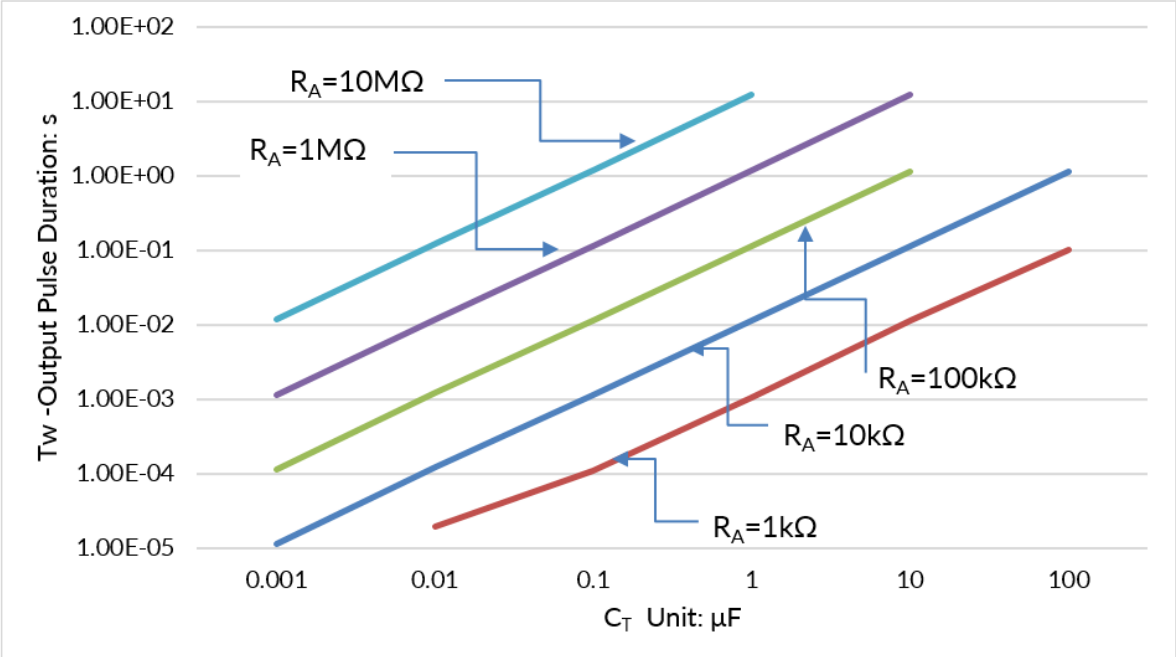


Figure 6. Output Pulse Duration vs Capacitance

11.2 A-stable Operation

As shown in Figure 7, adding a second resistor R_B, and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multi-vibrator. After the power supply is powered on or after the reset, capacitor C_T is charged by R_A and R_B and then discharged through R_B only. Therefore, the values of R_A and R_B can control the duty cycle. In the A steady-state circuit operation, the voltage on the capacitor C_T charges and discharges between the threshold voltage ($0.67*V_{DD}$) and the trigger voltage ($0.33*V_{DD}$). As with monostable circuits, the charging and discharge time (Frequency and duty cycle) are minimally affected by the power supply.

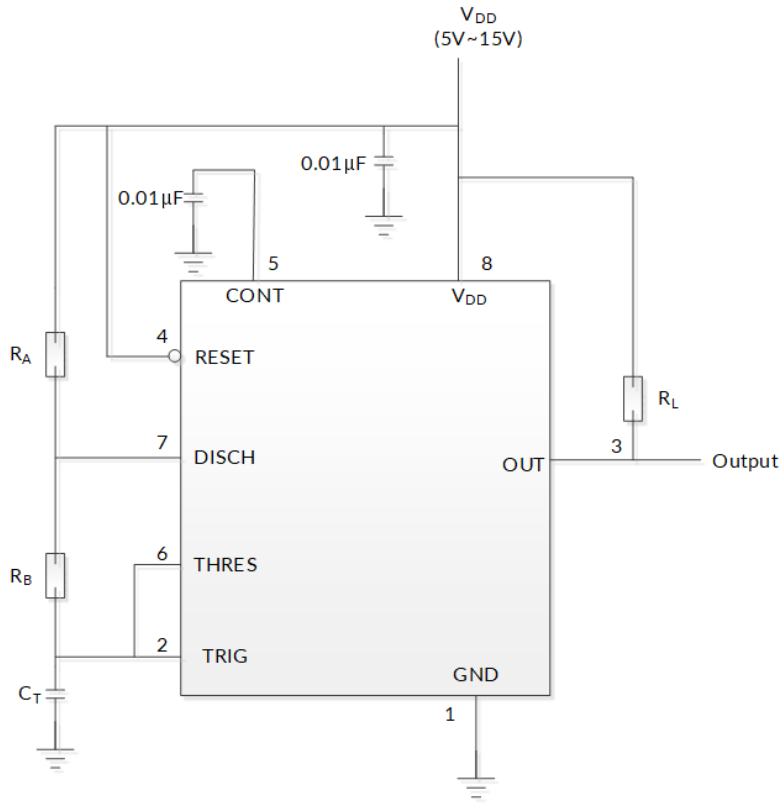


Figure 7. A stable Operation Circuit

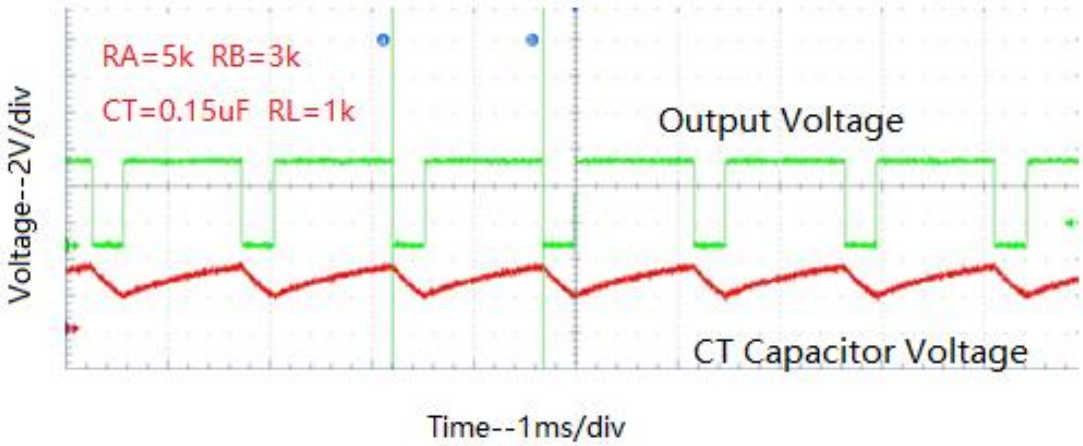


Figure 8. Typical Astable Waveforms

During astable operation, the output high-level duration T_H and low-level duration T_L can be calculated as follows:

$$T_H=0.693*（R_A+R_B）*C_T \quad (1)$$

$$T_L=0.693*R_B*C_T \quad (2)$$

Other useful relationships are shown below:

$$Period= T_H+ TL=0.693*（RA+2RB）*C_T \quad (3)$$

$$\text{frequency} = \frac{1.44}{(RA+2RB)CT} \quad (4)$$

$$\text{output waveform duty cycle}=\frac{TH}{TH+TL} = 1 - \frac{RB}{RA+2RB} \quad (5)$$

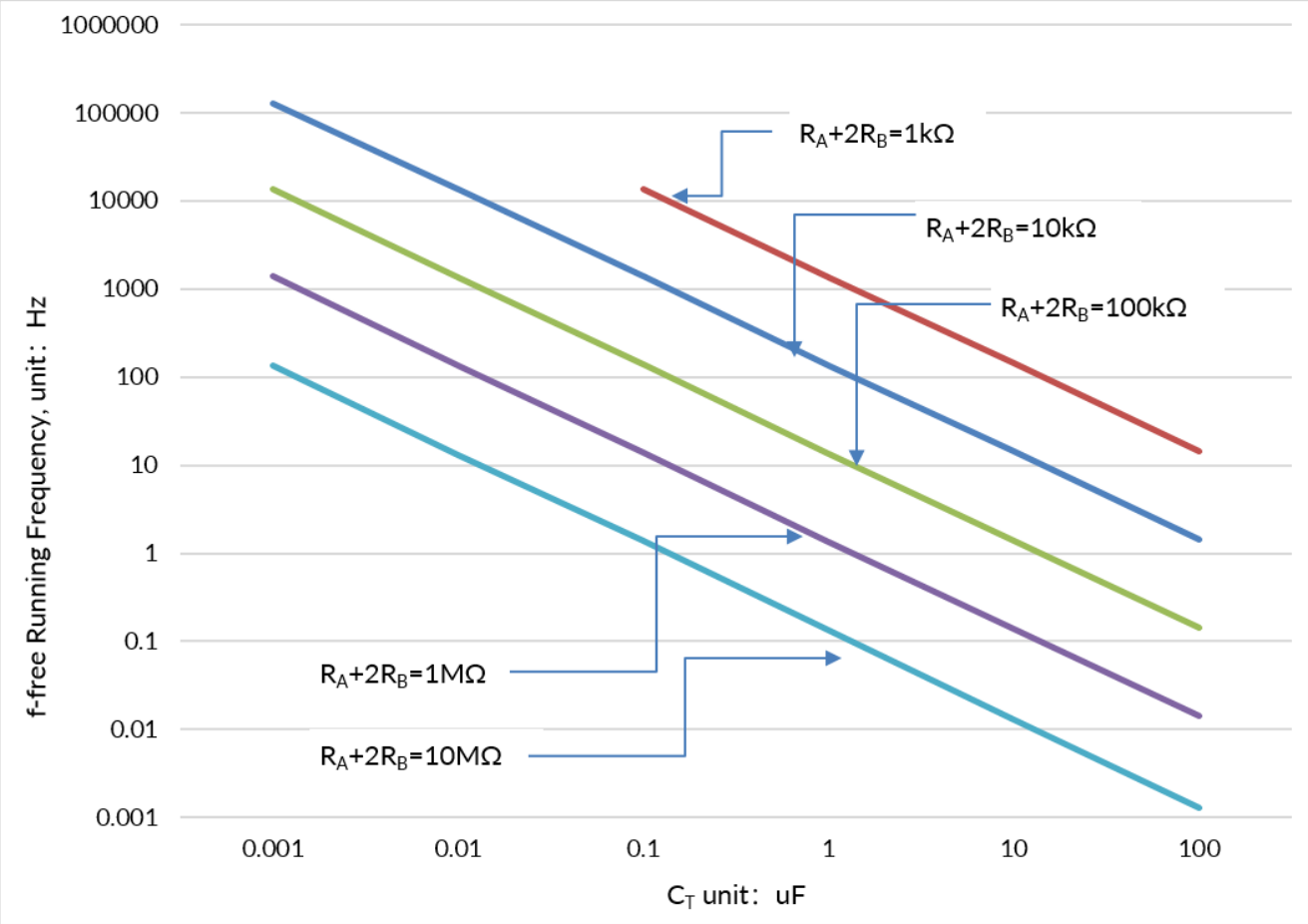


Figure 9. Free-Running Frequency

11.3 Frequency Divider

The Fig 4 circuit can be used as a frequency divider by properly config the peripheral device and adjusting the timing period of the trigger port. Figure 10 shows a three-frequency circuit waveform.

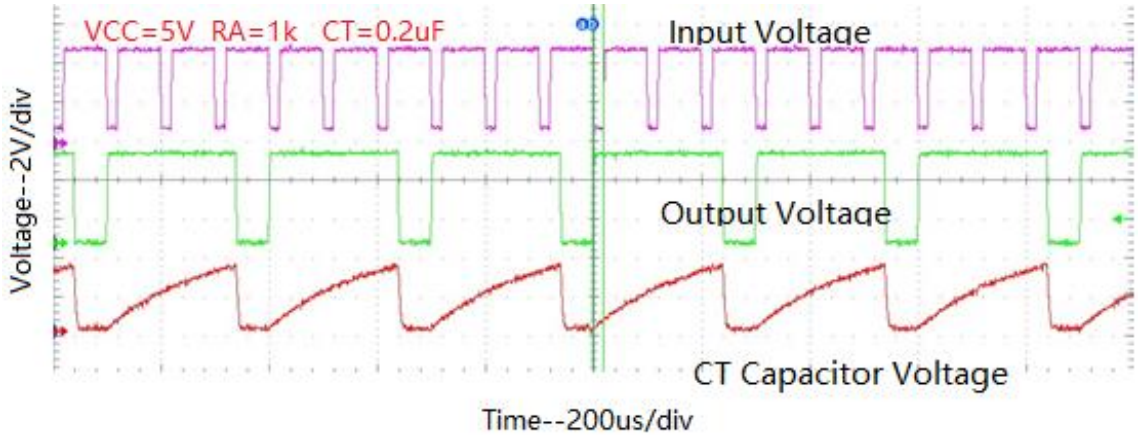


Figure 10. Divide-by-Three Circuit Waveforms

11.4 Pulse-Width Modulation

By adding an external voltage (such as sine wave) to the CONT, the threshold and trigger voltage inside the chip are modulated to achieve the operating state of the adjusted counter. Figure 11 shows the commonly used pulse width modulation circuit. A continuous input pulse train triggers a monostable circuit, and the CONT modulates the threshold voltage,the peak to peak value of the sine wave is 3.4v. The high level of the clock input at the TRIG must be greater than 1/3 VDD, and the low level must be less than 1/3 VDD. The frequency of the TRIG is 50kHz， the high level is 4v， the low level is 0v， the duty cycle is 75%,and the power supply is 5v.the results are shown in the figure 12.

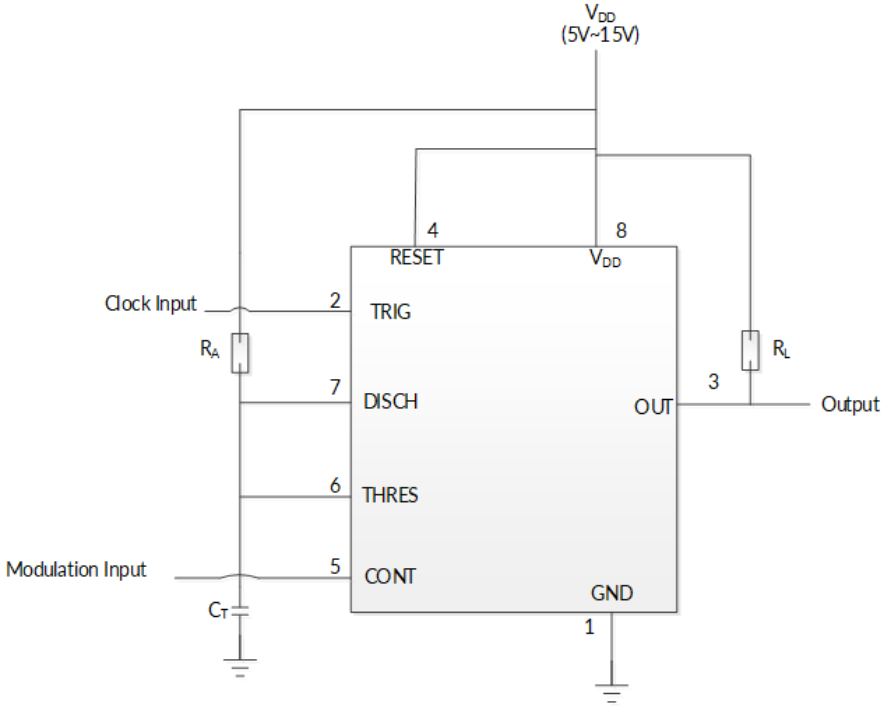


Figure 11. Circuit for Pulse-Width Modulation

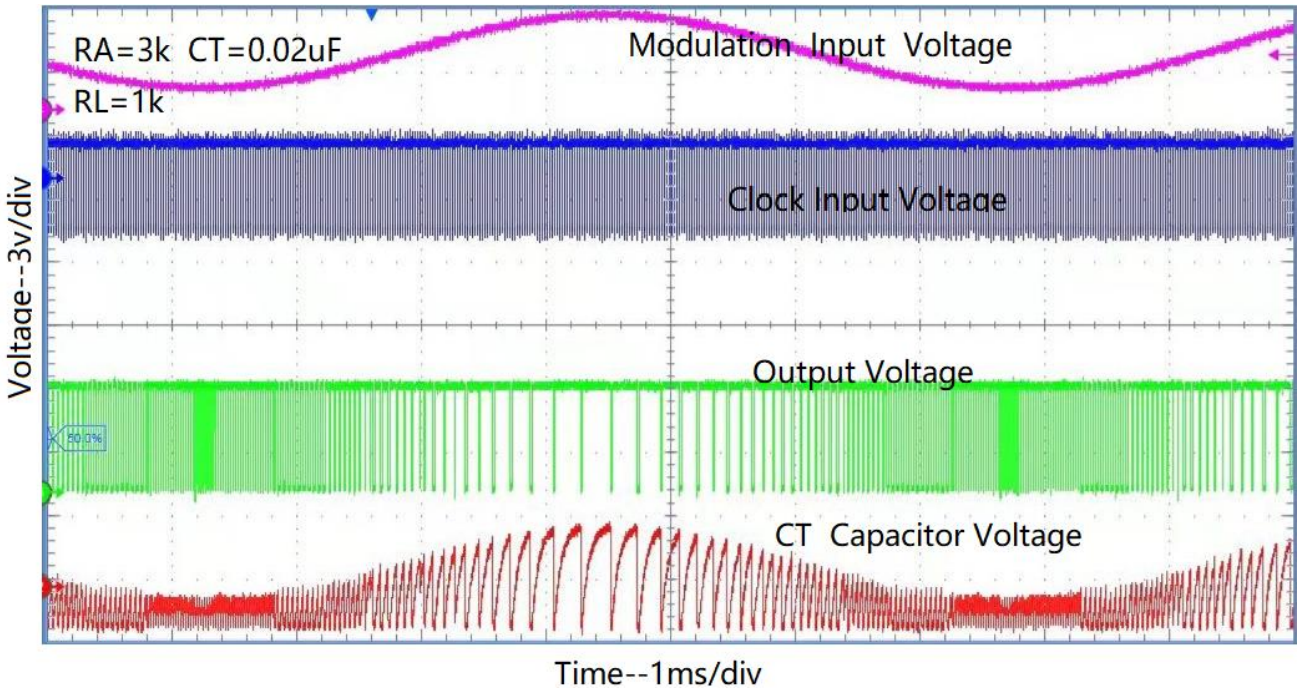


Figure 12. Pulse-Width-Modulatin Waveforms

11.5 Pulse-Position Modulation

As shown in Figure 13, in the free-running oscillator circuit, the corresponding output modulation waveform can be obtained by adding a modulation waveform to the CONT end.

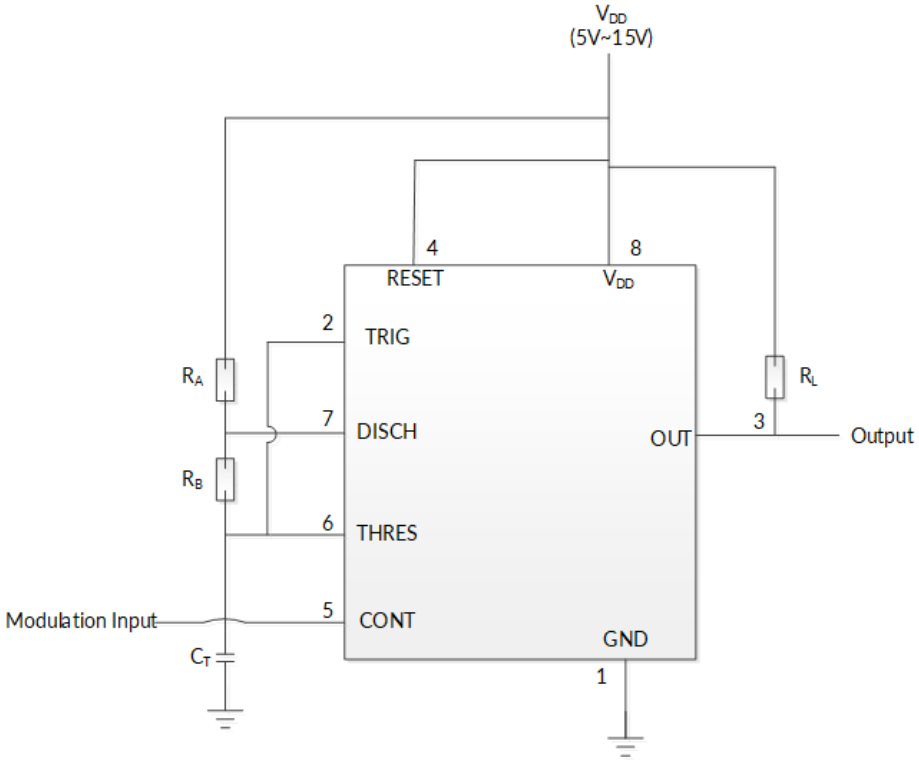


Figure 13. Circuit for Pulse-Position Modulation

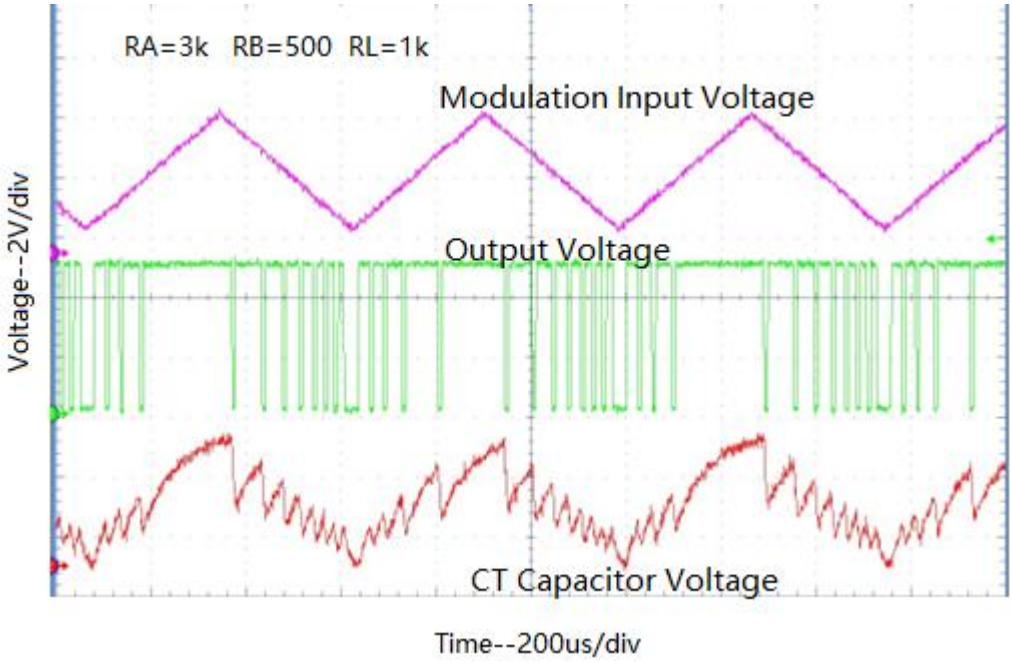


Figure 14. Pulse-Position-Modulation Waveforms

11.6 Sequential Timer

In many applications, signals are required to initialize conditions during startup. Timing control can be provided by connecting these timing circuits. These timers can be used with or without modulation in A variety of A-stable or monostable circuit connected combinatorial circuits to achieve waveform control. Figure 15 is one such application for a sequence generator circuit. In Figure 15, for example, the S-switch indicates that the input waveform can be a periodic square wave with a low pulse width of 0.1s and a period of 10s.

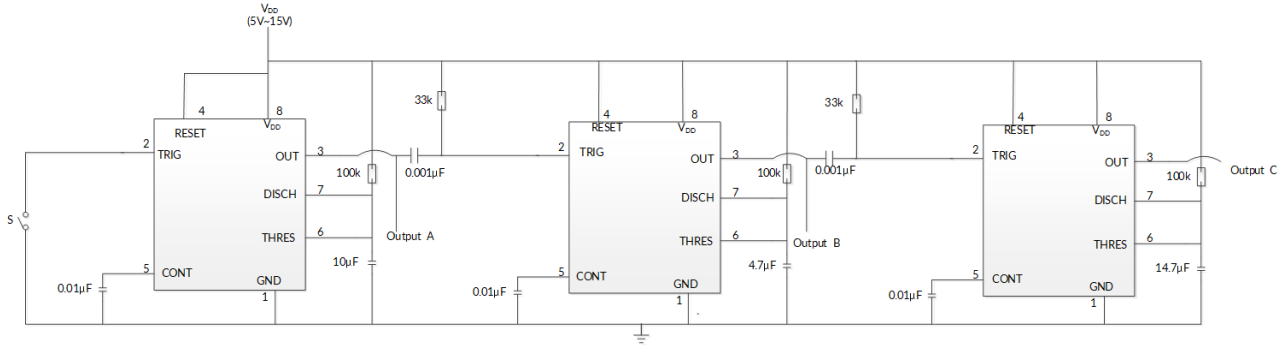


Figure 15. Sequential Timer Circuit

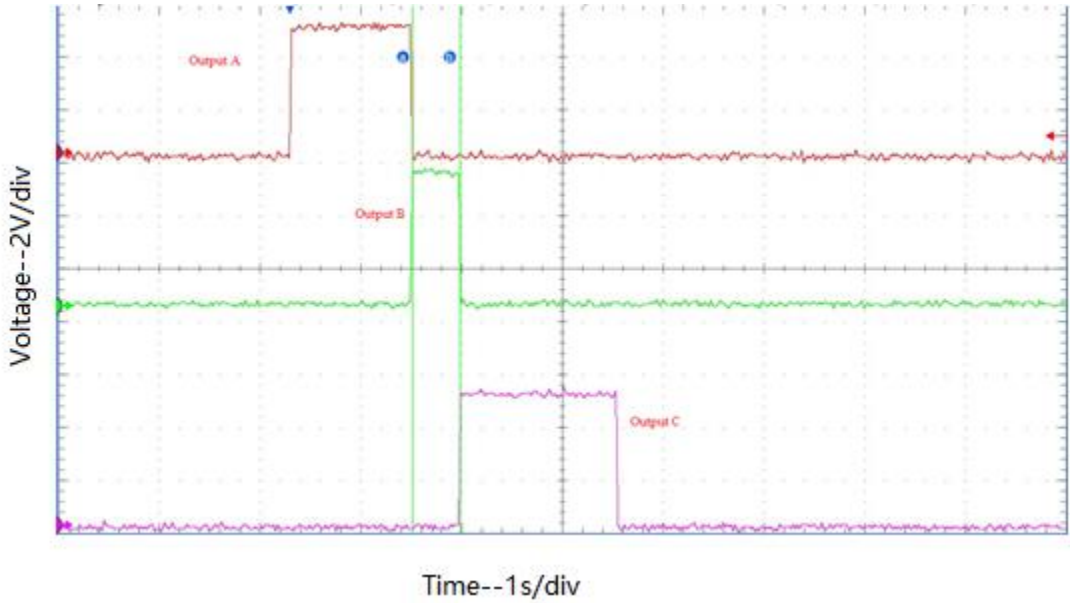


Figure 16. Sequential Timer Waveforms

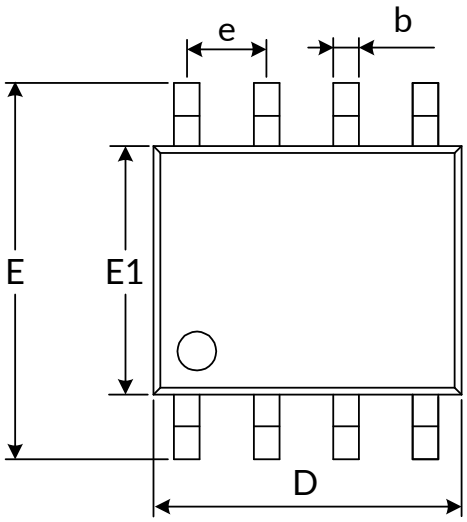
11.7 Device Functional Modes

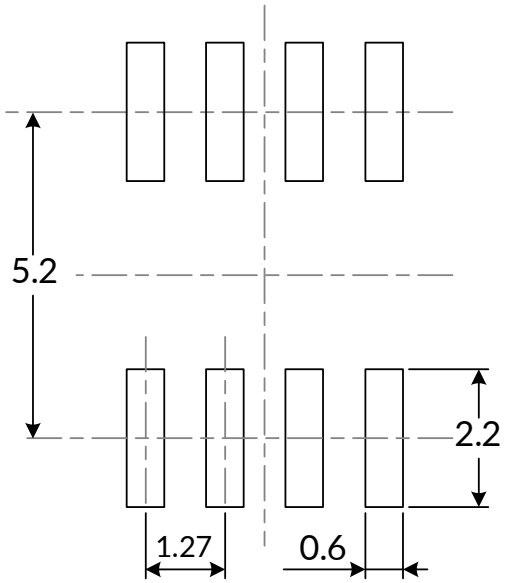
Table 6 Function Table

RESET	TRIGGER VOLTAGE (1)	THRESHOLD VOLTAGE (1)	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	<1/3 V_{cc}	Irrelevant	High	Off
High	>1/3 V_{cc}	>2/3 V_{cc}	Low	On
High	>1/3 V_{cc}	<2/3 V_{cc}	As previously established	

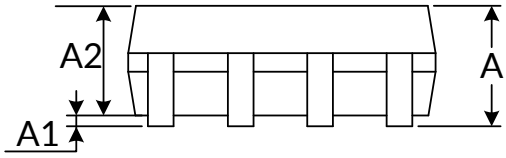
12 PACKAGE OUTLINE DIMENSIONS

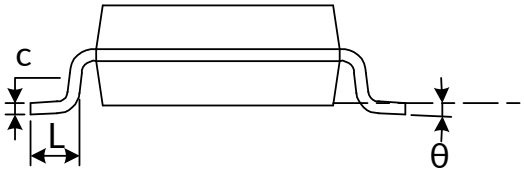
SOP8 (3)





RECOMMENDED LAND PATTERN (Unit: mm)



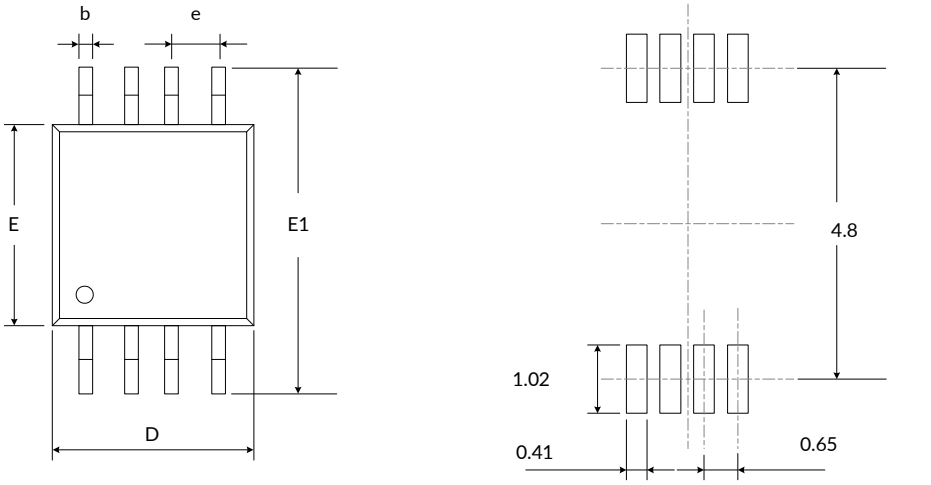


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D (1)	4.800	5.000	0.189	0.197
e	1.270(BSC) (2)		0.050(BSC) (2)	
E	5.800	6.200	0.228	0.244
E1 (1)	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

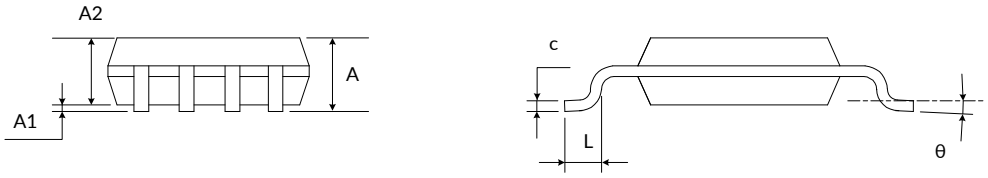
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

MSOP8 (3)



RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D (1)	2.900	3.100	0.114	0.122
e	0.650 (BSC) (2)		0.026 (BSC) (2)	
E (1)	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

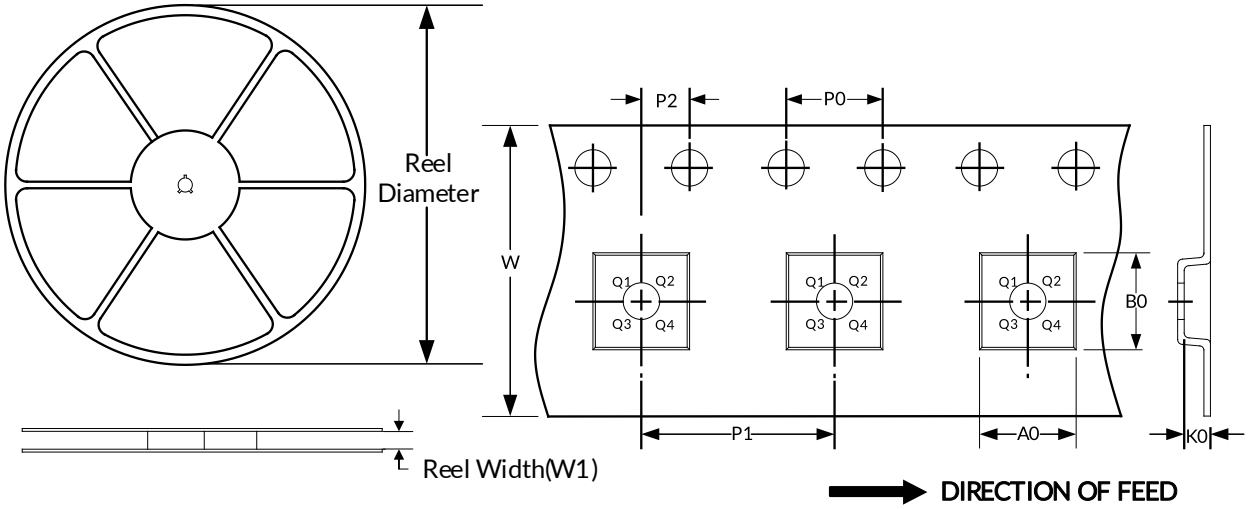
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

13 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOP8	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
MSOP8	13"	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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