16 Bit, 400KSPS, 2.7V to 5.5V, Analog-to-Digital Converter

1 FEATURES

- **16 Bits No Missing Codes (REF=2.5V)**
- **Very Low Noise (REF=2.5V): 33 µVrms**
- **Excellent Linearity (REF=2.5V):**
  - **±1.5LSB typ INL**
  - **±0.8LSB typ DNL**
  - **±0.5mV typ Offset**
  - **±3LSB typ Gain Error**
- **Micro Power:**
  - **12.5mW at 5V, 400KSPS**
  - **4.86mW at 2.7V, 300KSPS**
  - **1.62mW at 2.7V, 100KSPS**
  - **162µW at 2.7V, 10KSPS**
- **MSOP8 Packages**
- **SPI Interface**

2 APPLICATIONS

- **Automotive Navigation**
- **FA or ATM Equipment**
- **Industrial Controls**
- **Robotics**
- **Battery-Operated Systems**
- **Instrumentation and Control Systems**

3 DESCRIPTIONS

The RS1430A is a 16-bit analog-to-digital (A/D) converter specified for a supply voltage range from 2.7V to 5.5V. It requires very little power, even when operating at the full data rate. At lower data rates, the high speed of the device enables it to spend most of its time in the power-down mode. For example, the average power dissipation is less than 162µW at a 10kHz data rate.

The RS1430A offers excellent linearity and very low noise and distortion. It also features a synchronous serial (SPI/SSI-compatible) interface and a pseudo-differential input. The reference voltage can be set to any level within the range of 0.1V to VDD.

Low power and small size make the RS1430A ideal for portable and battery-operated systems. It is also a perfect fit for remote data-acquisition modules, simultaneous multichannel systems, and isolated data acquisition. The RS1430A is available in an MSOP8 package.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS1430A	MSOP8	3.00mm×3.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

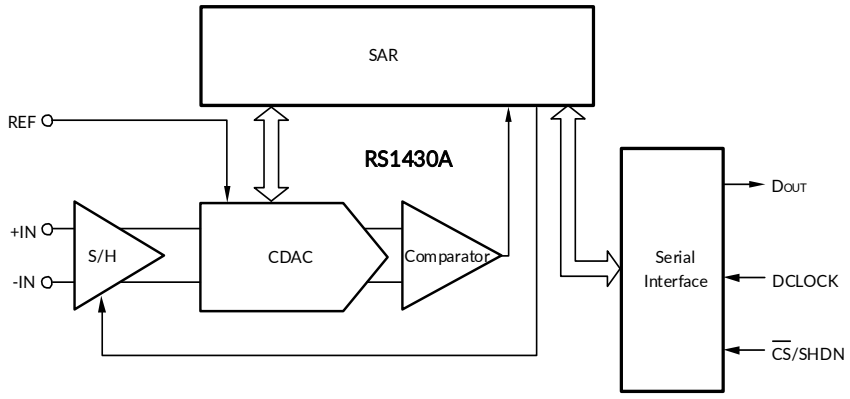


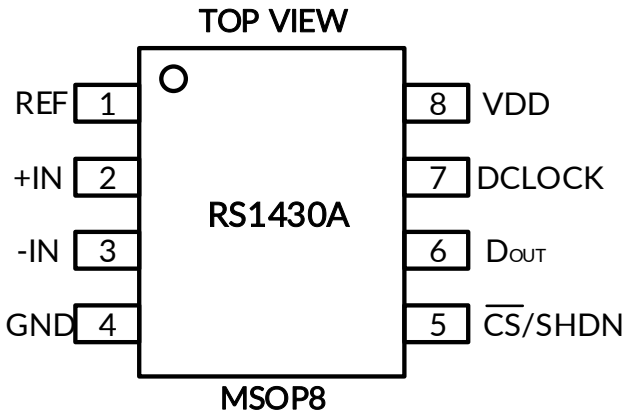
Table of Contents

4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2024/07/26	Preliminary version completed
A.1	2025/01/02	Initial version completed

5 PIN CONFIGURATION AND FUNCTIONS



PIN DESCRIPTION

NAME	PIN	I/O	DESCRIPTION
REF	1	Analog input	Reference input. It must be thoroughly bypassed.
+IN	2	Analog input	Noninverting analog input.
-IN	3	Analog input	Inverting analog input.
GND	4	Power-supply connection	The ground return for the supply.
$\overline{CS}$/SHDN	5	Digital input	Chip select when low; Shutdown mode when high.
DOUT	6	Digital output	Digital data output. The output words are clocked out of this pin by the DCLOCK pin.
DCLOCK	7	Digital input	Data clock synchronizes the serial data transfer and determines conversion speed.
VDD	8	Power-supply connection	Power supply. These pins must be connected to a quiet 2.7V to 5.5V source and bypassed to GND with 0.1μF and 1μF monolithic capacitors placed within 1 cm of the power pin.

6 SPECIFICATIONS

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Supply voltage, V_{DD} (2)			-0.3	6.5	V
Voltage on any analog pin to GND (2)			-0.3	V_{DD}+0.3	V
Voltage on any digital pin to GND (2)			-0.3	V_{DD}+0.3	V
Voltage on REF pin to GND (2)			-0.3	V_{DD}+0.2	V
Input current at any pin (except power supply pins)				±10	mA
θ_{JA}	Package thermal impedance (3)	MSOP8		206	°C/W
Soldering temperature, infrared (10 sec)				215	°C
Operating temperature, T_A			-40	125	°C
Storage temperature, T_{stg}			-65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Analog input terminal is diode-clamped to the power-supply rails. Input signal that can swing more than 0.3V beyond the supply rails should be current-limited to 10mA or less.
(3) The package thermal impedance is calculated in accordance with JESD-51.

6.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-Device Model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±1500	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	2.7		5.5	V
REF	Reference input voltage	0.1		V_{DD}	
+IN/-IN	–IN to GND	-0.3	0	0.5	
	+IN to GND	-0.3		V_{DD}+0.2	
	+IN – (–IN)	0		V_{REF}	
T_A	Operating temperature	-40		125	°C

6.4 Electrical Characteristics: V_{DD} = +5V

At –40°C to +125°C, V_{REF} = +5V, –IN = GND, F_S = 400kHz, and f_{DCLOCK}= 24 × F_S, typical values are at T_A = 25°C, unless otherwise noted. (1)(2)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}			V_{REF}-0.2		5.5	V
STATIC CONVERTER CHARACTERISTICS						
NMC	No Missing Codes		15			Bits
INL	Integral Non-Linearity		-3	±1.5	+3	LSB
DNL	Differential Non-Linearity		-1	-0.9/1.5	+3	LSB
V_{OS}	Offset Error			±0.5		mV
TCV_{OS}	Offset Error Drift			±0.5		ppm/°C
GE	Gain Error			±2		LSB
TCGE	Gain Error Drift			±1		ppm/°C
TUE	Total Unadjusted Error			±5		LSB
	Noise			45		µVrms
				5		LSB_{PP}
DYNAMIC CONVERTER CHARACTERISTICS (3)						
ENOB	Effective Number of Bits	f_{IN}=2kHz		14.66		Bits
		f_{IN}=10kHz		14.49		Bits
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN}=2kHz		90		dB
		f_{IN}=10kHz		89		dB
SNR	Signal-to-Noise Ratio	f_{IN}=2kHz		90.5		dB
		f_{IN}=10kHz		90		dB
THD	Total Harmonic Distortion	f_{IN}=2kHz		-100		dB
		f_{IN}=10kHz		-95		dB
SFDR	Spurious-Free Dynamic Range	f_{IN}=2kHz		101		dB
		f_{IN}=10kHz		98		dB
FPBW	60dB SINAD Bandwidth	5V supply		700		kHz
PSRR	Power-Supply Rejection	4.75V ≤ V_{DD} ≤ 5.25V		0.6		LSB/V
ANALOG INPUT CHARACTERISTICS						
FSR	Full-Scale Range	+IN – (-IN)	0		V_{REF}	V
	Common-Mode Signal	-IN	-0.3		0.5	V
C_{IN}	Input Capacitance	-IN = GND, during sampling		48		pF
I_{IL}	Input Leakage Current	$\overline{CS}$/SHDN=V_{DD}, SCLK off		±0.1		µA

(1) Data sheet minimum and maximum specification limits are ensured by design, test, or statistical analysis.
(2) Applies for 5.0V nominal supply: V_{DD} (min) = 4.5V and V_{DD} (max) = 5.5V.
(3) All ac parameters are tested at -0.2 dBFs.

Electrical Characteristics: V_{DD} = +5V (continued)

At –40°C to +125°C, V_{REF} = +5V, –IN = GND, F_S = 400kHz, and f_{DCLOCK} = 24 × F_S, typical values are at T_A = 25°C, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE INPUT CHARACTERISTICS						
V_{REF}	Reference Voltage		0.1		V_{DD}	V
C_{REF}	Reference Input Capacitance			48		pF
I_{REF}	Reference Input Current	F_S =400KSPS		200		µA
		F_S =300KSPS		150		µA
		F_S =250KSPS		125		µA
		F_S =200KSPS		100		µA
		F_S =100KSPS		50		µA
		F_S=10KSPS		5		µA
		$\overline{CS}$/SHDN=V_{DD}		±1		µA
SAMPLING DYNAMIC CHARACTERISTICS						
t_{CONV}	Conversion Time	24kHz ≤ f_{DCLOCK} ≤ 9.6MHz	16			T_{DCLOCK}
t_{AQ}	Acquisition Time		4.5	5		T_{DCLOCK}
Fs	Throughput Rate	24kHz ≤ f_{DCLOCK} ≤ 9.6MHz			400	KSPS
f_{DCLOCK}	Clock Frequency		0.024		9.6	MHz
POWER SUPPLY CHARACTERISTICS						
I_{VDD}	Operating Supply Current	f_{DCLOCK}=9.6MHz, F_S=400KSPS		2.5	3	mA
		f_{DCLOCK}=9.6MHz, F_S=300KSPS		1.8		mA
		f_{DCLOCK}=9.6MHz, F_S=200KSPS		1.2		mA
	Power-Down Supply Current	$\overline{CS}$/SHDN=V_{DD}, SCLK Off		0.1		µA
P_{VDD}	Operating Power Dissipation	f_{DCLOCK}=9.6MHz, F_S=400KSPS		12.5	15	mW
		f_{DCLOCK}=9.6MHz, F_S=300KSPS		9		mW
		f_{DCLOCK}=9.6MHz, F_S=200KSPS		6		mW
	Power Dissipation In Power-Down	$\overline{CS}$/SHDN=V_{DD}, SCLK Off		0.5		µW
DIGITAL INPUT CHARACTERISTICS						
	Logic Family		CMOS			
V_{IH}	Input High Voltage		0.7V_{DD}		V_{DD}+0.3	V
V_{IL}	Input Low Voltage		-0.3		0.3V_{DD}	V
C_{IN}	Input Capacitance			5		pF
I_{IN}	Input Current			±0.1		µA
DIGITAL OUTPUT CHARACTERISTICS						
	Logic Family		CMOS			
	Data Format		Straight binary			
V_{OH}		I_{OH} = -100µA	V_{DD}-0.3			V
V_{OL}		I_{OL} = 100µA			0.3	V
I_{OZ}	High-Impedance State Output Current	$\overline{CS}$/SHDN = V_{DD}, V_I = V_{DD} or GND		±0.1		µA
C_O	Output Capacitance			5		pF
C_L	Load Capacitance				30	pF

6.5 Electrical Characteristics: V_{DD} = +5V

At –40°C to +125°C, V_{REF} = +2.5V, –IN = GND, F_S = 400kHz, and f_{DCLOCK}= 24 × F_S, typical values are at T_A = 25°C, unless otherwise noted. (1)(2)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}			4.5		5.5	V
STATIC CONVERTER CHARACTERISTICS						
NMC	Resolution with No Missing Codes		16			Bits
INL	Integral Non-Linearity		-2	±1	+2	LSB
DNL	Differential Non-Linearity		-0.99	±0.8	+2	LSB
V_{OS}	Offset Error		-1	±0.5	+1	mV
TCV_{OS}	Offset Error Drift			±0.65		ppm/°C
GE	Gain Error		-24	±3	+24	LSB
TCGE	Gain Error Drift			±1.3		ppm/°C
TUE	Total Unadjusted Error			±8		LSB
	Noise			35		µVrms
				7		LSB_{PP}
DYNAMIC CONVERTER CHARACTERISTICS (3)						
ENOB	Effective Number of Bits	f_{IN}=2kHz	13.5	14.1		Bits
		f_{IN}=10kHz		14.05		Bits
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN}=2kHz	83	87		dB
		f_{IN}=10kHz		86.5		dB
SNR	Signal-to-Noise Ratio	f_{IN}=2kHz	84	87		dB
		f_{IN}=10kHz		87		dB
THD	Total Harmonic Distortion	f_{IN}=2kHz		-100	-94	dB
		f_{IN}=10kHz		-97		dB
SFDR	Spurious-Free Dynamic Range	f_{IN}=2kHz	95	103		dB
		f_{IN}=10kHz		101		dB
FPBW	60dB SINAD Bandwidth	5V supply		700		kHz
PSRR	Power-Supply Rejection	4.75V ≤ V_{DD} ≤ 5.25V		1.6		LSB/V
ANALOG INPUT CHARACTERISTICS						
FSR	Full-Scale Range	+IN – (-IN)	0		V_{REF}	V
	Common-Mode Signal	-IN	-0.3		0.5	V
C_{IN}	Input Capacitance	-IN = GND, during sampling		48		pF
I_{IL}	Input Leakage Current	$\overline{CS}$/SHDN=V_{DD}, SCLK off	-1	±0.1	+1	µA

(1) Data sheet minimum and maximum specification limits are ensured by design, test, or statistical analysis.
(2) Applies for 5.0V nominal supply: V_{DD} (min) = 4.5V and V_{DD} (max) = 5.5V.
(3) All ac parameters are tested at -0.2 dBFs.

Electrical Characteristics: V_{DD} = +5V (continued)

At –40°C to +125°C, V_{REF} = +2.5V, –IN = GND, F_S = 400kHz, and f_{DCLOCK} = 24 × F_S, typical values are at T_A = 25°C, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE INPUT CHARACTERISTICS						
V_{REF}	Reference Voltage		0.1		V_{DD}	V
C_{REF}	Reference Input Capacitance			48		pF
I_{REF}	Reference Input Current	F_S =400KSPS		96		µA
		F_S =300KSPS		72		µA
		F_S =250KSPS		60		µA
		F_S =200KSPS		48		µA
		F_S =100KSPS		24		µA
		F_S=10KSPS		2.4		µA
		$\overline{CS}$/SHDN=V_{DD}	-5	±1	+5	µA
SAMPLING DYNAMIC CHARACTERISTICS						
t_{CONV}	Conversion Time	24kHz ≤ f_{DCLOCK} ≤ 9.6MHz	16			T_{DCLOCK}
t_{AQ}	Acquisition Time		4.5	5		T_{DCLOCK}
Fs	Throughput Rate	24kHz ≤ f_{DCLOCK} ≤ 9.6MHz			400	KSPS
f_{DCLOCK}	Clock Frequency		0.024		9.6	MHz
POWER SUPPLY CHARACTERISTICS						
I_{VDD}	Operating Supply Current	f_{DCLOCK}=9.6MHz, F_S=400KSPS		2.5	3	mA
		f_{DCLOCK}=9.6MHz, F_S=200KSPS		1.2		mA
		f_{DCLOCK}=9.6MHz, F_S=100KSPS		0.6		mA
	Power-Down Supply Current	$\overline{CS}$/SHDN=V_{DD}, SCLK Off		0.1		µA
P_{VDD}	Operating Power Dissipation	f_{DCLOCK}=9.6MHz, F_S=400KSPS		12.5	15	mW
		f_{DCLOCK}=9.6MHz, F_S=200KSPS		6		mW
		f_{DCLOCK}=9.6MHz, F_S=100KSPS		3		mW
	Power Dissipation In Power-Down	$\overline{CS}$/SHDN=V_{DD}, SCLK Off		0.5		µW
DIGITAL INPUT CHARACTERISTICS						
	Logic Family		CMOS			
V_{IH}	Input High Voltage		0.7V_{DD}		V_{DD}+0.3	V
V_{IL}	Input Low Voltage		-0.3		0.3V_{DD}	V
C_{IN}	Input Capacitance			5		pF
I_{IN}	Input Current		-1	±0.1	+1	µA
DIGITAL OUTPUT CHARACTERISTICS						
	Logic Family		CMOS			
	Data Format		Straight binary			
V_{OH}		I_{OH} = -100µA	V_{DD}-0.3			V
V_{OL}		I_{OL} = 100µA			0.3	V
I_{OZ}	High-Impedance State Output Current	$\overline{CS}$/SHDN = V_{DD}, V_I = V_{DD} or GND	-1	±0.1	+1	µA
C_O	Output Capacitance			5		pF
C_L	Load Capacitance				30	pF

6.6 Electrical Characteristics: V_{DD} = +2.7V

At –40°C to +125°C, V_{REF} = +2.5V, –IN = GND, F_S = 300kHz, and f_{DCLOCK} = 24 × F_S, typical values are at T_A = 25°C, unless otherwise noted. (1)(2)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}			2.7		3.6	V
STATIC CONVERTER CHARACTERISTICS						
NMC	Resolution with No Missing Codes		16			Bits
INL	Integral Non-Linearity		-2.5	±1.5	+2.5	LSB
DNL	Differential Non-Linearity		-0.99	±0.9	+2.5	LSB
V_{OS}	Offset Error			±0.5		mV
TCV_{OS}	Offset Error Drift			±1		ppm/°C
GE	Gain Error			±3		LSB
TCGE	Gain Error Drift			±0.4		ppm/°C
TUE	Total Unadjusted Error			±10		LSB
	Noise			33		µVrms
				7		LSB_{PP}
DYNAMIC CONVERTER CHARACTERISTICS (3)						
ENOB	Effective Number of Bits	f_{IN}=2kHz		14.2		Bits
		f_{IN}=10kHz		14.1		Bits
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN}=2kHz		87		dB
		f_{IN}=10kHz		86		dB
SNR	Signal-to-Noise Ratio	f_{IN}=2kHz		87		dB
		f_{IN}=10kHz		86.5		dB
THD	Total Harmonic Distortion	f_{IN}=2kHz		-100		dB
		f_{IN}=10kHz		-95		dB
SFDR	Spurious-Free Dynamic Range	f_{IN}=2kHz		101		dB
		f_{IN}=10kHz		96		dB
FPBW	60dB SINAD Bandwidth	2.7V supply		700		kHz
PSRR	Power-Supply Rejection	2.7V ≤ V_{DD} ≤ 3.6V		1		LSB/V
ANALOG INPUT CHARACTERISTICS						
FSR	Full-Scale Range	+IN – (-IN)	0		V_{REF}	V
	Common-Mode Signal	-IN	-0.3		0.5	V
C_{IN}	Input Capacitance	-IN = GND, during sampling		48		pF
I_{IL}	Input Leakage Current	$\overline{CS}$/SHDN=V_{DD}, SCLK off		±0.1		µA

(1) Data sheet minimum and maximum specification limits are ensured by design, test, or statistical analysis.
(2) Applies for 2.7V nominal supply: V_{DD} (min) = 2.7V and V_{DD} (max) = 3.6V.
(3) All ac parameters are tested at -0.2 dBFs.

Electrical Characteristics: V_{DD} = +2.7V (continued)

At –40°C to +125°C, V_{REF} = +2.5V, –IN = GND, F_S = 300kHz, and f_{DCLOCK} = 24 × F_S, typical values are at T_A = 25°C, unless otherwise noted.

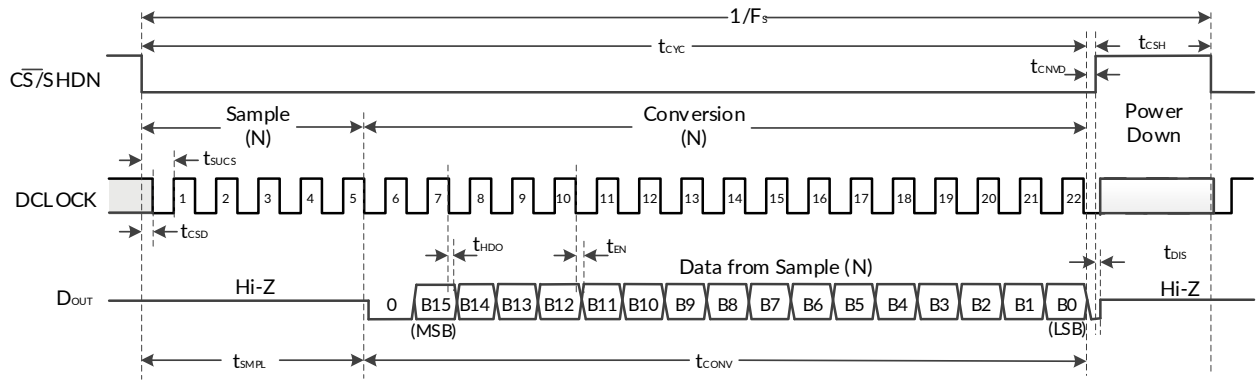
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE INPUT CHARACTERISTICS						
V_{REF}	Reference Voltage		0.1		V_{DD}	V
C_{REF}	Reference Input Capacitance			48		pF
I_{REF}	Reference Input Current	Fs=300KSPS		72		µA
		Fs=250KSPS		60		µA
		Fs=100KSPS		24		µA
		Fs=10KSPS		2.4		µA
		$\overline{CS}$/SHDN=V_{DD}		±1		µA
SAMPLING DYNAMIC CHARACTERISTICS						
t_{CONV}	Conversion Time	24kHz ≤ f_{DCLOCK} ≤ 7.2MHz	16			T_{DCLOCK}
t_{AQ}	Acquisition Time		4.5	5		T_{DCLOCK}
F_S	Throughput Rate	24kHz ≤ f_{DCLOCK} ≤ 7.2MHz			300	KSPS
f_{DCLOCK}	Clock Frequency		0.024		7.2	MHz
POWER SUPPLY CHARACTERISTICS						
I_{VDD}	Operating Supply Current	f_{DCLOCK} =7.2MHz, F_S=300KSPS		1.8		mA
		f_{DCLOCK} =7.2MHz, F_S=200KSPS		1.2		mA
		f_{DCLOCK} =7.2MHz, F_S=100KSPS		0.6		mA
		f_{DCLOCK} =7.2MHz, F_S=10KSPS		0.06		mA
	Power-Down Supply Current	$\overline{CS}$/SHDN=V_{DD}, SCLK Off		0.1		µA
P_{VDD}	Operating Power Dissipation	f_{DCLOCK} =7.2MHz, F_S=300KSPS		4.86		mW
		f_{DCLOCK} =7.2MHz, F_S=200KSPS		3.24		mW
		f_{DCLOCK} =7.2MHz, F_S=100KSPS		1.62		mW
		f_{DCLOCK} =7.2MHz, F_S=10KSPS		162		µW
	Power Dissipation in Power-Down	$\overline{CS}$/SHDN=V_{DD}, SCLK Off		0.27		µW
DIGITAL INPUT CHARACTERISTICS						
	Logic Family		CMOS			
V_{IH}	Input High Voltage		0.7V_{DD}		V_{DD}+0.3	V
V_{IL}	Input Low Voltage		-0.3		0.3V_{DD}	V
C_{IN}	Input Capacitance			5		pF
I_{IN}	Input Current			±0.1		µA
DIGITAL OUTPUT CHARACTERISTICS						
	Logic Family		CMOS			
	Data Format		Straight binary			
V_{OH}		I_{OH} = -100µA	V_{DD}-0.3			V
V_{OL}		I_{OL} = 100µA			0.3	V
I_{OZ}	High-Impedance State Output Current	$\overline{CS}$/SHDN = V_{DD}, V_I = V_{DD} or GND		±0.1		µA
C_O	Output Capacitance			5		pF
C_L	Load Capacitance				30	pF

6.7 Timing Requirements

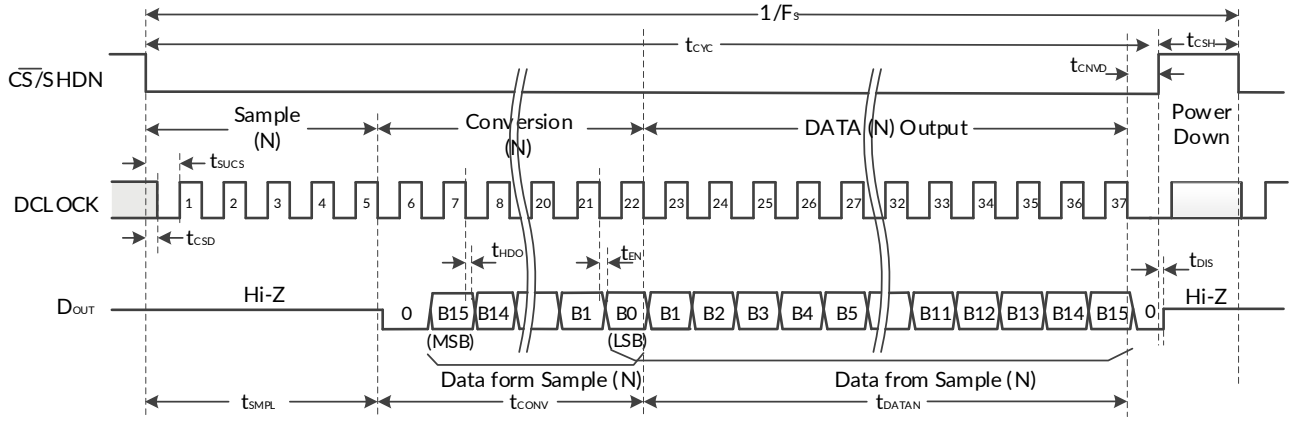
-40°C ≤ T_A ≤ 125°C, V_{DD} = 2.7 V to 5.5 V (unless otherwise noted) (1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
f_{DCLOCK}	DCLOCK Frequency	V_{DD} = 4.5V to 5.5V			9.6	MHz
		V_{DD} = 2.7V to 3.6V			7.2	MHz
F_S	Throughput Rate	V_{DD} = 4.5V to 5.5V			400	KSPS
		V_{DD} = 2.7V to 3.6V			300	KSPS
t_{SMPL}	Analog Input Sample Time		4.5		5	DCLOCKs
t_{CONV}	Conversion Time		16			DCLOCKs
t_{CYC}	Complete Cycle Time		22			DCLOCKs
t_{CSH}	Minimum CS Pulse Width		10			ns
t_{CSD}	CS Falling to DCLOCK Low				0	ns
t_{SUCS}	CS Falling to DCLOCK Rising		20			ns
t_{HDO}	DCLOCK Falling to Current D_{OUT} Not Valid			15		ns
t_{DIS}	CS Rising to D_{OUT} Tri-State				100	ns
t_{EN}	DCLOCK Falling to D_{OUT} Enabled				50	ns
t_{CNVD}	The 22rd DCLOCK Falling to CS Rising		50			ns
t_F	D_{OUT} Fall Time				40	ns
t_R	D_{OUT} Rise Time				40	ns
t_{WH}	Pulse Duration, DCLOCK High		40			ns
t_{WL}	Pulse Duration, DCLOCK Low		40			ns
t_{AD}	Aperture Delay			7.5		ns
t_{AJ}	Aperture Jitter			30		ns

(1) Measured with 20pF load.



NOTE: (1) A minimum of 22 clock cycles are required for 16-bit conversion; 24 clock cycles are shown.
If $\overline{CS}$/SHDN remains low at the end of conversion, a new data stream from sample (N) is shifted out.



NOTE: (2) After completing the data transfer, if further clocks are applied with CS low, the A/D converter will output data(n) repeatedly.

Figure 1. RS1430A Serial Interface Timing Diagram

6.8 Typical Characteristics: V_{DD} = +5V

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

T_A = 25°C, V_{DD} = +5 V, V_{REF} = +5 V, F_S = 400 KSPS, $f_{DCLOCLK}$ = 9.6 MHz, f_{IN}= 2.07 kHz, P_{IN}= -0.2 dBFs (unless otherwisenoted).

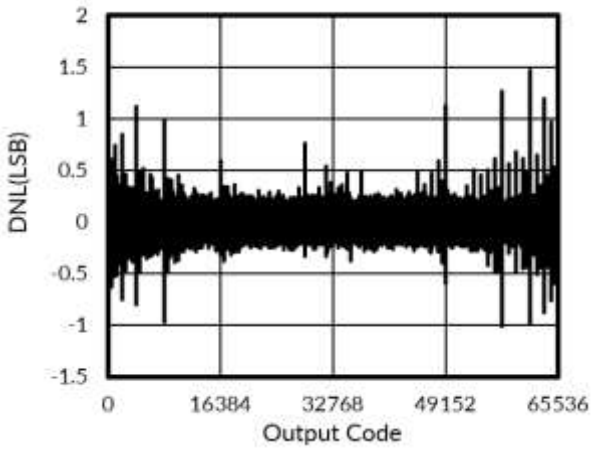


Figure 2. DNL vs Output Code

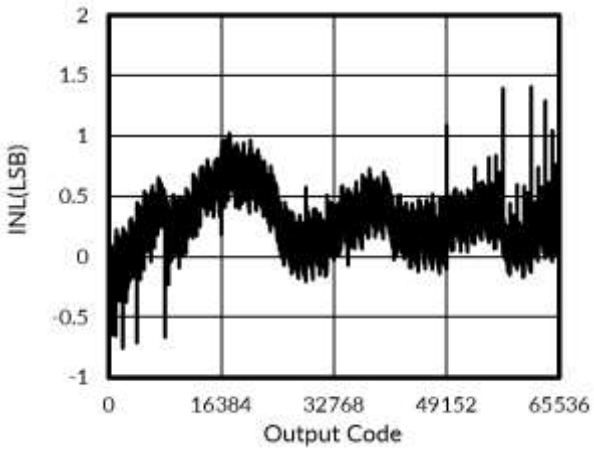


Figure 3. INL vs Output Cod

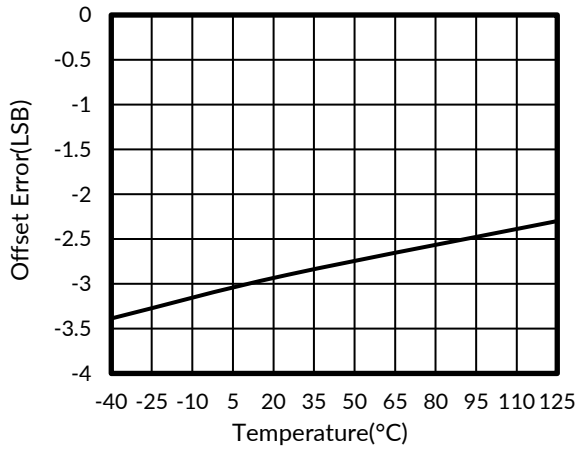


Figure 4. Offset Error vs Temperature

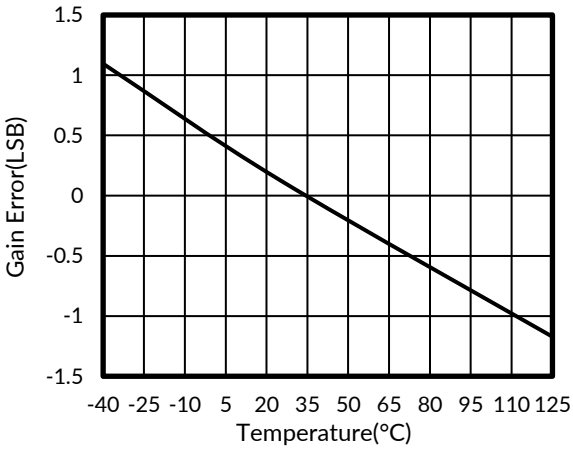


Figure 5. Gain Error vs Temperature

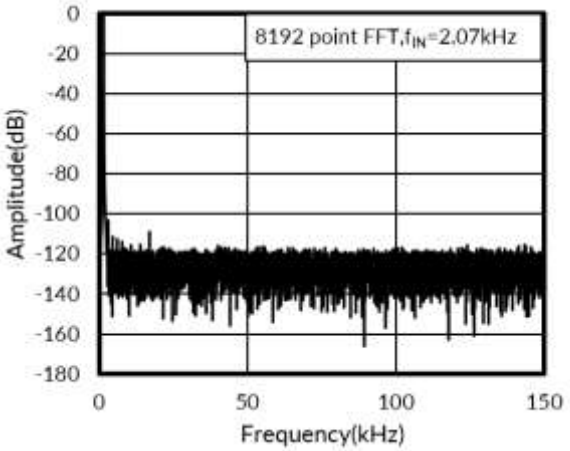


Figure 6. Spectral Response

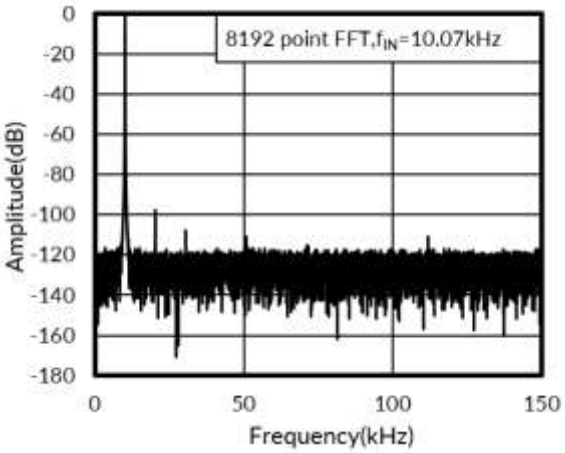


Figure 7. Spectral Response

Typical Characteristics: V_{DD} = +5V (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

T_A = 25°C, V_{DD} = +5 V, V_{REF} = +5 V, F_S = 400 KSPS, $f_{DCLOCLK}$ = 9.6 MHz, f_{IN}= 2.07 kHz, P_{IN}= -0.2 dBFs (unless otherwisenoted).

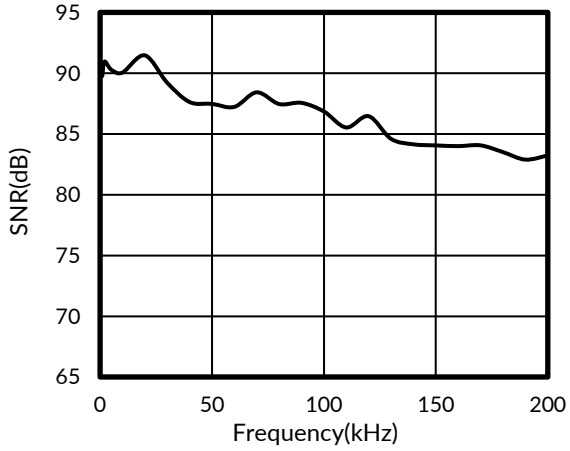


Figure 8. SNR vs Input Frequency

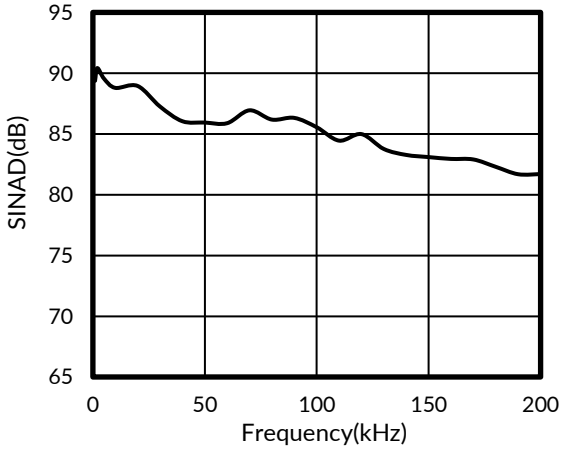


Figure 9. SINAD vs Input Frequency

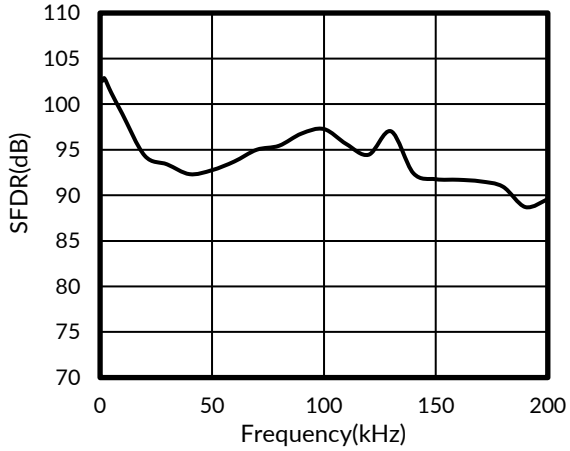


Figure 10. SFDR vs Input Frequency

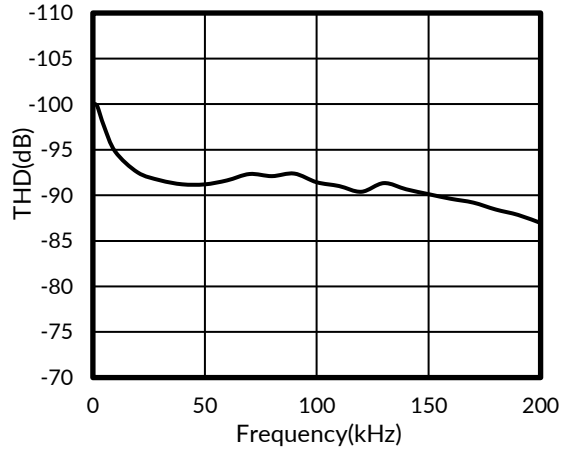


Figure 11. THD vs Input Frequency

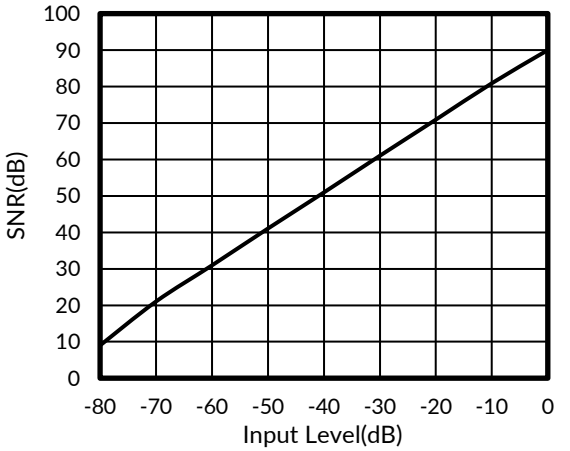


Figure 12. SNR vs Input Level

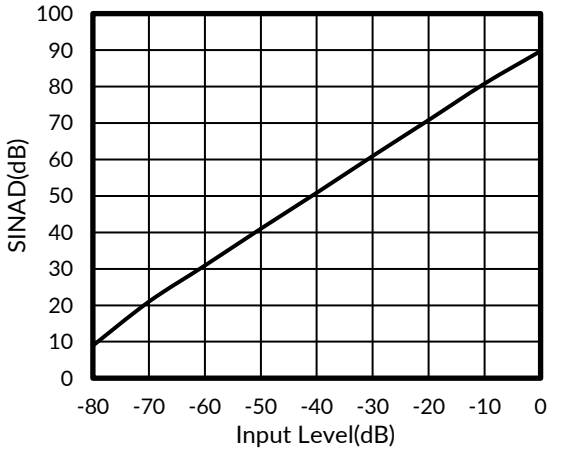


Figure 13. SINAD vs Input Level

Typical Characteristics: V_{DD} = +5V (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

T_A = 25°C, V_{DD} = +5 V, V_{REF} = +5 V, F_S = 400 KSPS, $f_{DCLOCLK}$ = 9.6 MHz, f_{IN}= 2.07 kHz, P_{IN}= -0.2 dBFs (unless otherwisenoted).

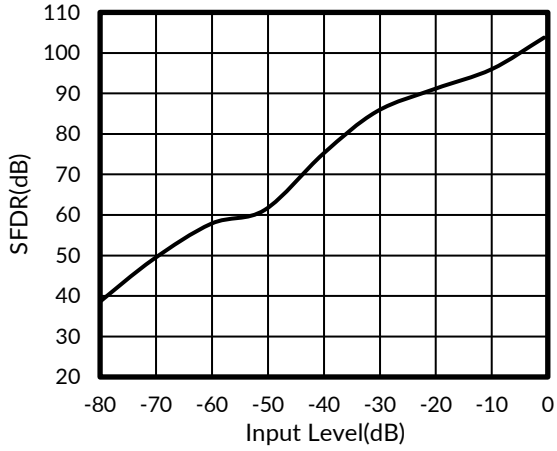


Figure 14. SFDR vs Input Level

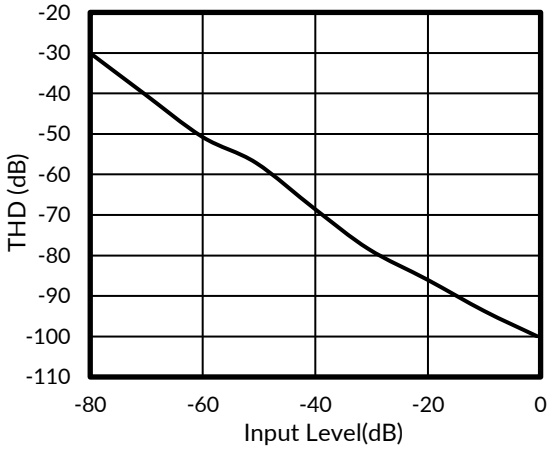


Figure 15. THD vs Input Level

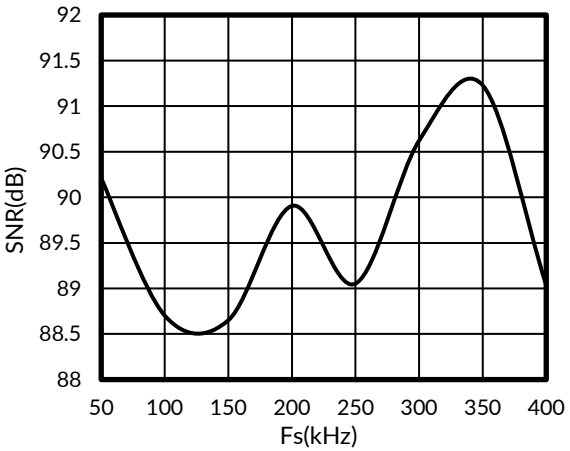


Figure 16. SNR vs Fs

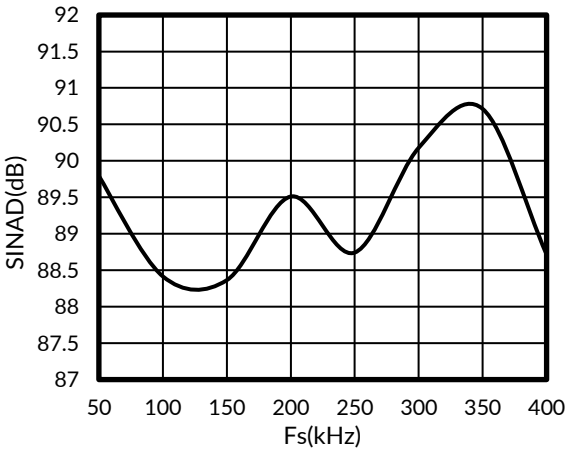


Figure 17. SINAD vs Fs

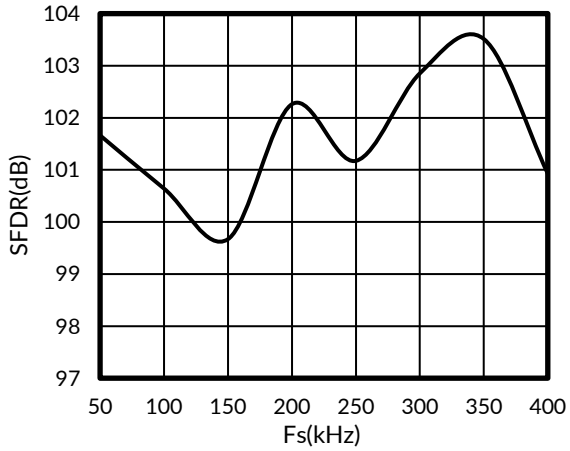


Figure 18. SFDR vs Fs

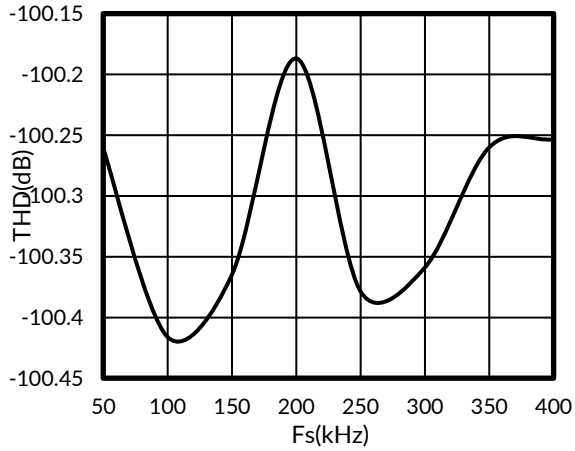


Figure 19. THD vs Fs

Typical Characteristics: V_{DD} = +5V (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

T_A = 25°C, V_{DD} = +5 V, V_{REF} = +5 V, F_S = 400 KSPS, $f_{DCLOCLK}$ = 9.6 MHz, f_{IN}= 2.07 kHz, P_{IN}= -0.2 dBFs (unless otherwisenoted).

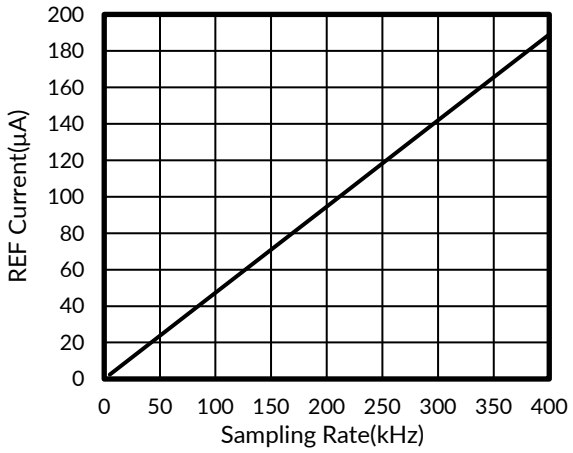


Figure 20. REF Current vs Sampling Rate

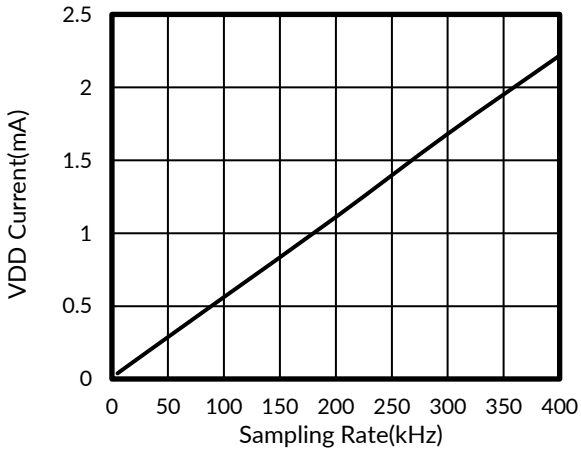


Figure 21. VDD Current vs Sampling Rate

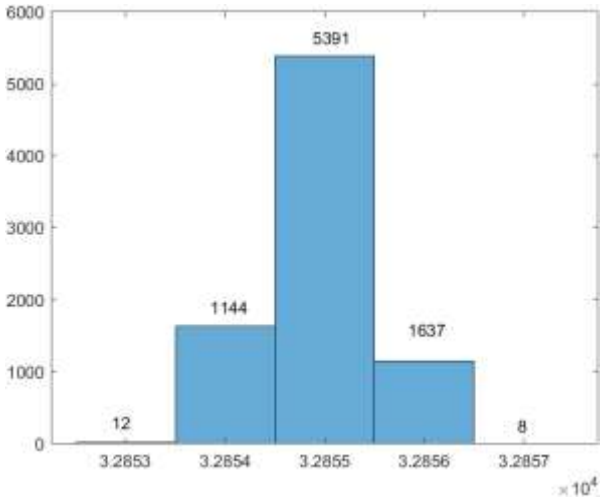


Figure 22. Output Code Histogram from a DC Input (8192 Conversions)

6.9 Typical Characteristics: V_{DD} = +2.7V

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

T_A = 25°C, V_{DD} = +2.7 V, V_{REF} = +2.5 V, F_S = 300 KSPS, $f_{DCLOCLK}$ = 7.2 MHz, f_{IN} = 2.07 kHz, P_{IN} = -0.2 dBFs (unless otherwise noted).

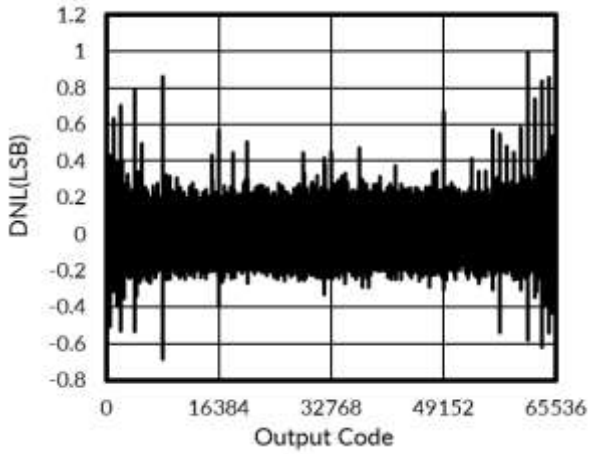


Figure 23. DNL vs Output Code

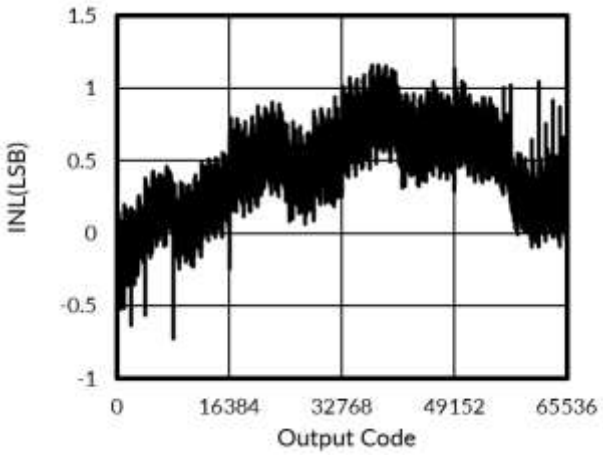


Figure 24. INL vs Output Code

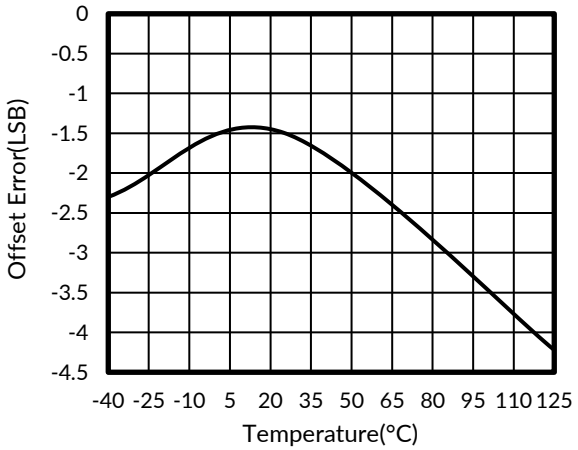


Figure 25. Offset Error vs Temperature

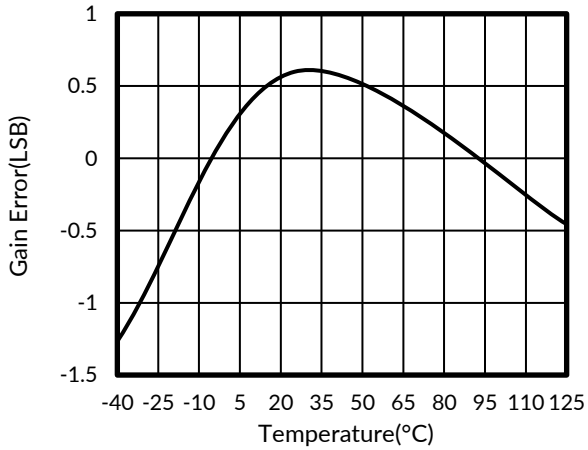


Figure 26. Gain Error vs Temperature

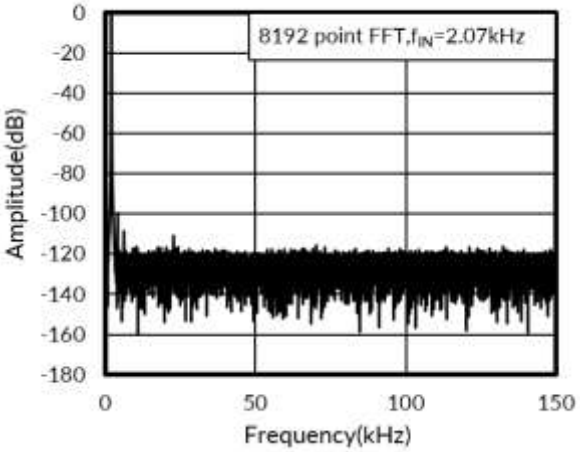


Figure 27. Spectral Response

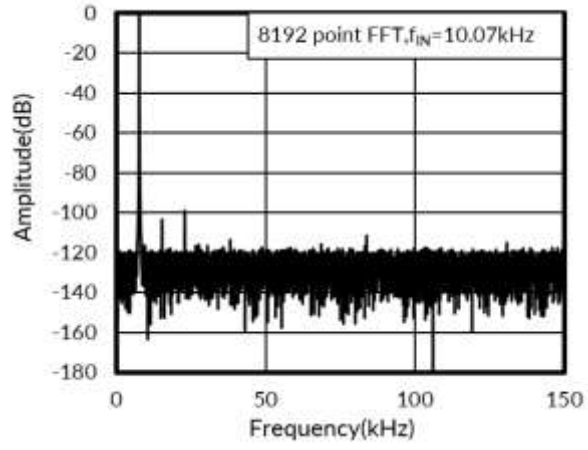


Figure 28. Spectral Response

Typical Characteristics: V_{DD} = +2.7V (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

T_A = 25°C, V_{DD} = +2.7 V, V_{REF} = +2.5 V, F_S = 300 KSPS, $f_{DCLOCLK}$ = 7.2 MHz, f_{IN} = 2.07 kHz, P_{IN} = -0.2 dBFs (unless otherwise noted).

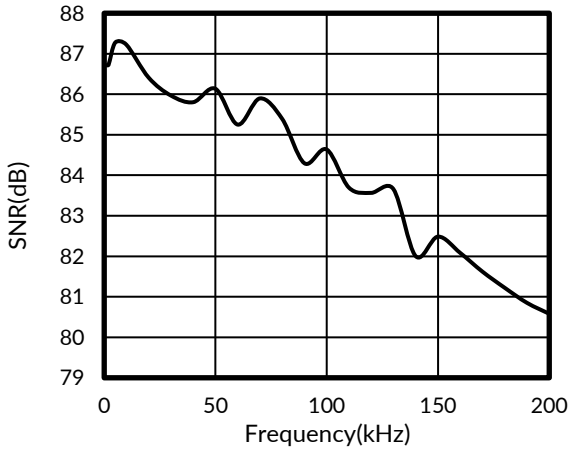


Figure 29. SNR vs Input Frequency

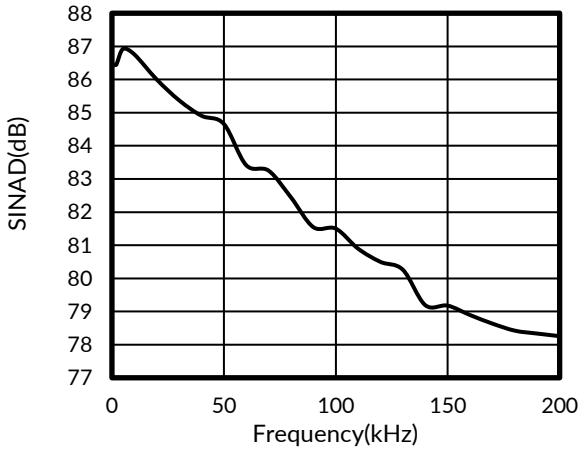


Figure 30. SINAD vs Input Frequency

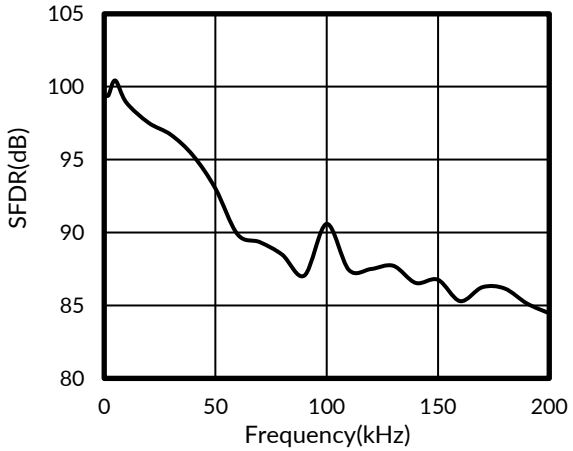


Figure 31. SFDR vs Input Frequency

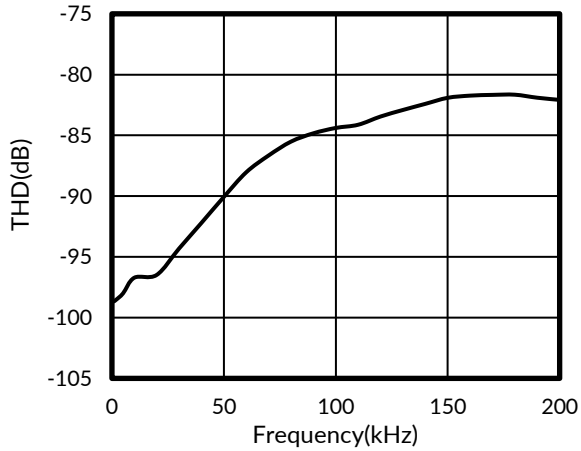


Figure 32. THD vs Input Frequency

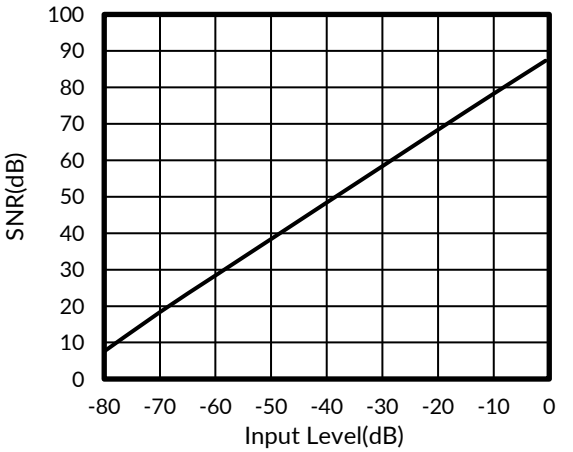


Figure 33. SNR vs Input Level

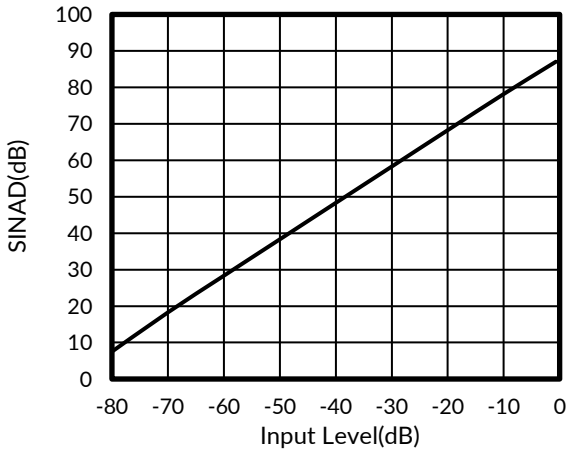


Figure 34. SINAD vs Input Level

Typical Characteristics: V_{DD} = +2.7V (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

T_A = 25°C, V_{DD} = +2.7 V, V_{REF} = +2.5 V, F_S = 300 KSPS, $f_{DCLOCLK}$ = 7.2 MHz, f_{IN} = 2.07 kHz, P_{IN} = -0.2 dBFs (unless otherwise noted).

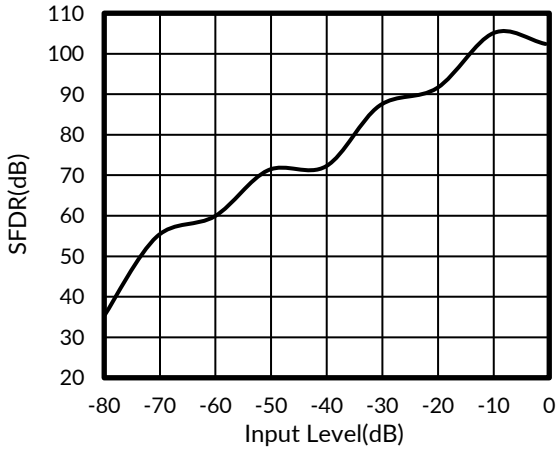


Figure 35. SFDR vs Input Level

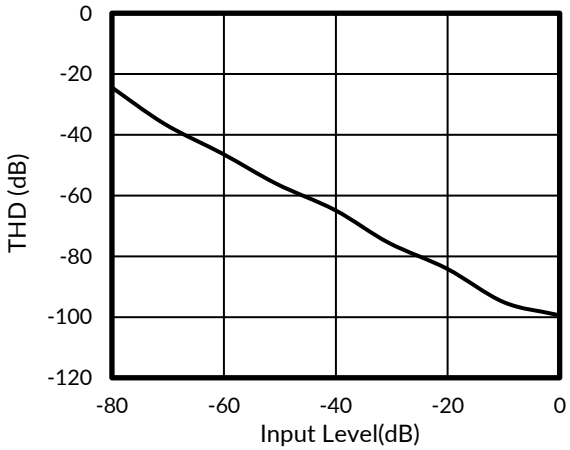


Figure 36. THD vs Input Level

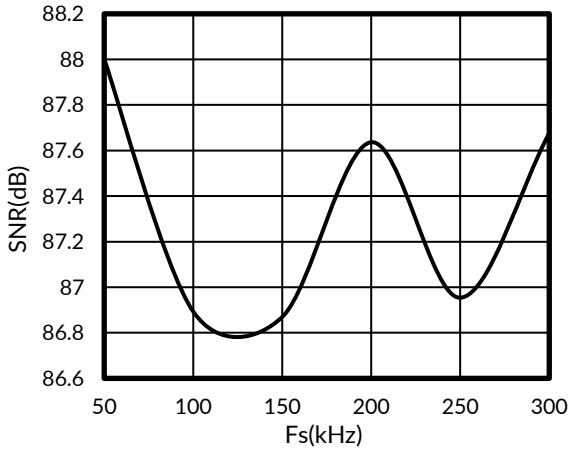


Figure 37. SNR vs Fs

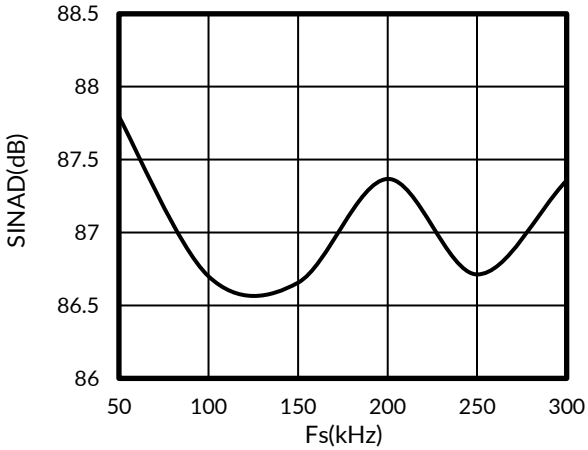


Figure 38. SINAD vs Fs

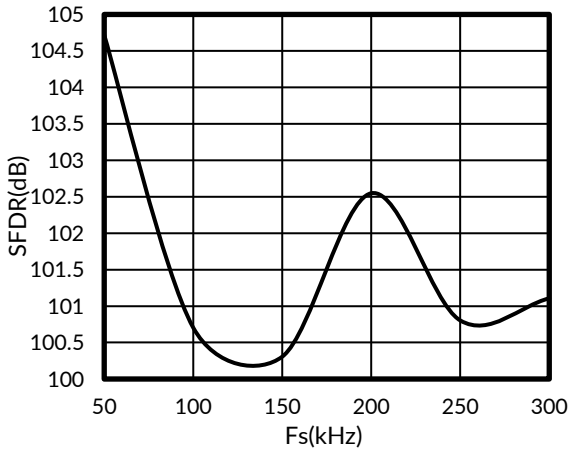


Figure 39. SFDR vs Fs

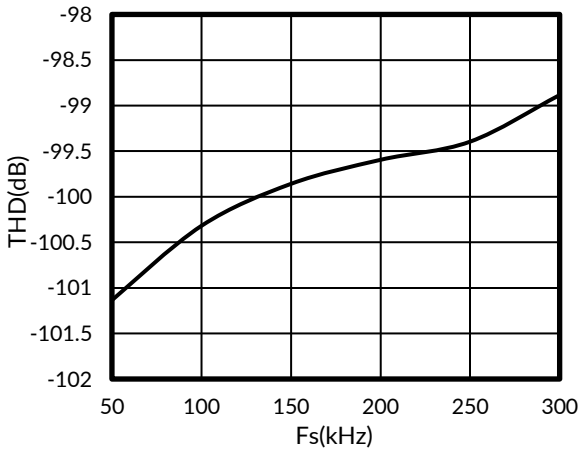


Figure 40. THD vs Fs

Typical Characteristics: V_{DD} = +2.7V (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

T_A = 25°C, V_{DD} = +2.7 V, V_{REF} = +2.5 V, F_S = 300 KSPS, $f_{DCLOCLK}$ = 7.2 MHz, f_{IN} = 2.07 kHz, P_{IN} = -0.2 dBFs (unless otherwise noted).

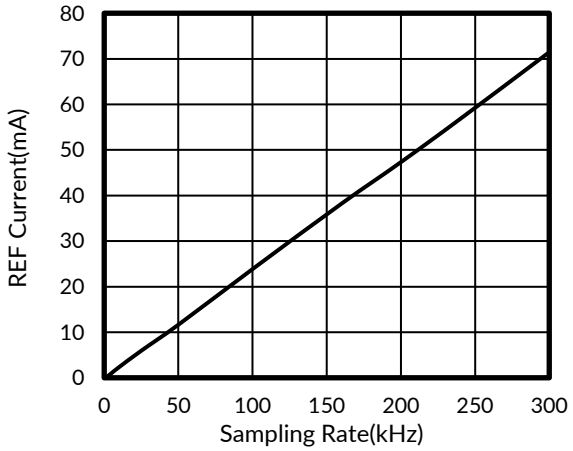


Figure 41. REF Current vs Sampling Rate

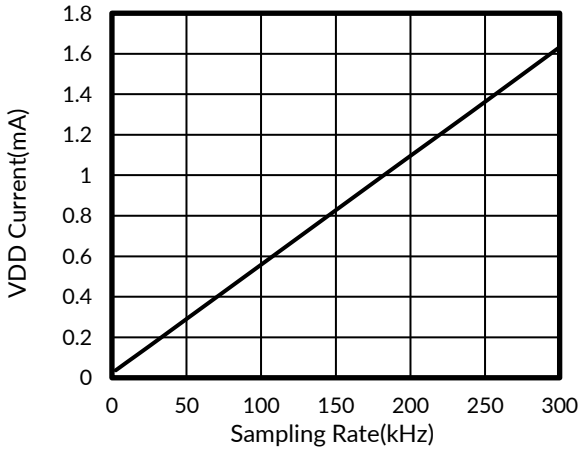


Figure 42. VDD Current vs Sampling Rate

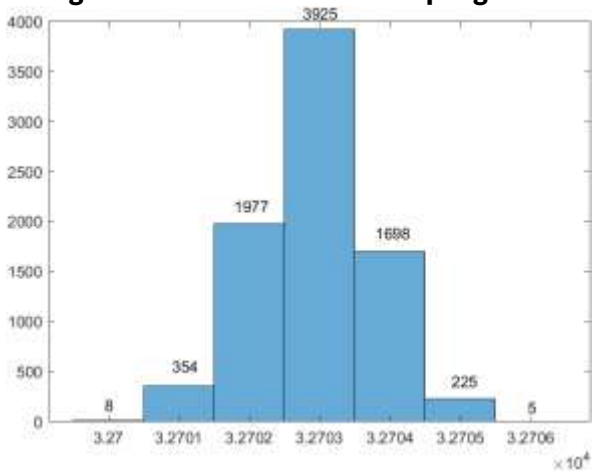


Figure 43. Output Code Histogram from a DC Input (8192 Conversions)

7 DETAILED DESCRIPTION

7.1 Overview

The RS1430A device is a classic successive approximation register (SAR) analog-to-digital (A/D) converter. The architecture is based on capacitive redistribution, which inherently includes a sample and hold function. The architecture and process allow the RS1430A to acquire and convert an analog signal at up to 400,000 conversions per second while consuming less than 12mW from V_{DD}.

Differential linearity for the RS1430A is factory-adjusted via a package-level trim procedure. The state of the trim elements is stored in non-volatile memory and is continuously updated after each acquisition cycle, just prior to the start of the successive approximation operation. This process ensures that one complete conversion cycle always returns the part to its factory-adjusted state in the event of a power interruption.

The RS1430A requires an external reference, an external clock, and a single power source (V_{DD}). The external reference can be any voltage between 0.1 V and V_{DD}. The value of the reference voltage directly sets the range of the analog input. The reference input current depends on the conversion rate of the RS1430A.

The external clock can vary between 24 kHz (1-kHz throughput) and 9.6 MHz (400-kHz throughput). The duty cycle of the clock is essentially unimportant, as long as the minimum high and low times are at least 40 ns (V_{DD} = 2.7 V or greater). The minimum clock frequency is set by the leakage on the internal capacitors to the RS1430A.

The analog input is provided to two input pins: +IN and -IN. When a conversion is initiated, the pseudo-differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

The digital result of the conversion is clocked out by the DCLOCK input and is provided serially, most significant bit first, on the D_{OUT} pin. The digital data that is provided on the D_{OUT} pin is for the conversion currently in progress (no pipeline delay). It is possible to continue to clock the RS1430A after the conversion is complete and to obtain the serial data least significant bit first. See the Timing Information section for more information.

7.2 Analog Input

The analog input of RS1430A is pseudo-differential. The +IN and -IN input pins allow for a pseudo-differential input signal. The amplitude of the input is the difference between the +IN and -IN input, or (+IN) - (-IN). Unlike some converters of this type, the -IN input is not resampled later in the conversion cycle. When the converter goes into Hold mode or conversion, the voltage difference between +IN and -IN is captured on the internal capacitor array.

The range of the -IN input is limited to -0.3V to +0.5V. As a result of this limitation, the pseudo-differential input could be used to reject signals that are common to both inputs in the specified range. Thus, the -IN input is best used to sense a remote signal ground that may move slightly with respect to the local ground potential.

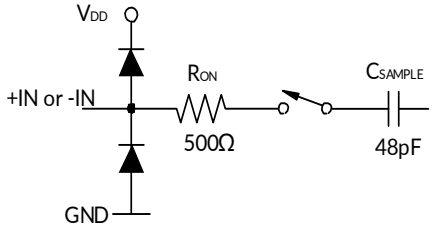


Figure 44. Equivalent Analog Input Circuit of RS1430A

The general method for driving the analog input of the RS1430A is shown in **Figure 44** and **Figure 45**. The -IN input is held at the common-mode voltage. The +IN input swings from -IN (or common-mode voltage) to -IN +V_{REF} (or common-mode voltage +V_{REF}), and the peak-to-peak amplitude is +V_{REF}. The value of V_{REF} determines the range over which the common-mode voltage may vary, as shown in **Figure 46**.

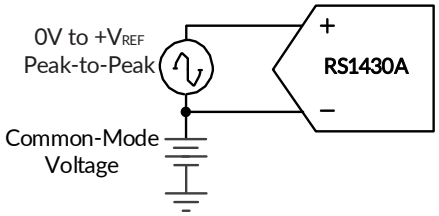


Figure 45. Methods of Driving the RS1430A

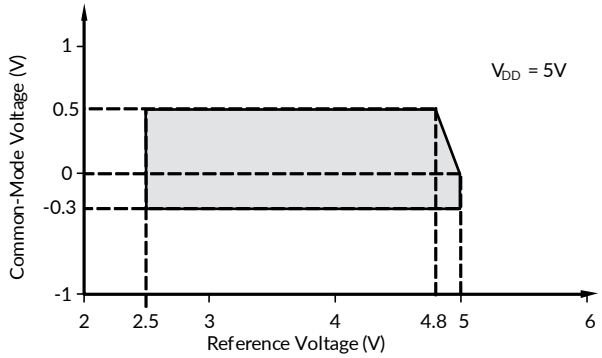
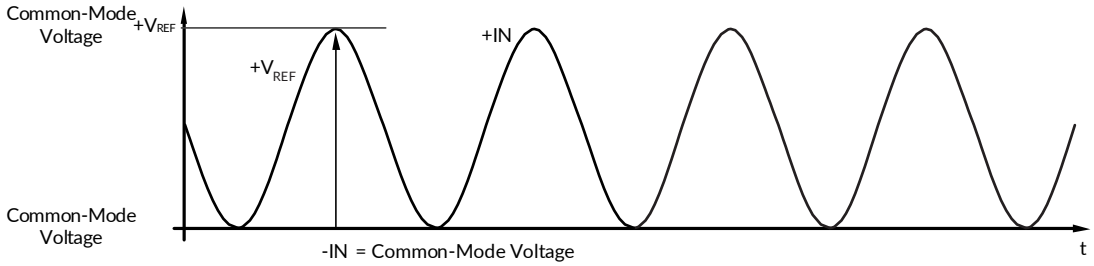


Figure 46. -IN Analog Input: Common-Mode Voltage Range vs V_{REF}



NOTE: The maximum differential voltage between +IN and -IN of the RS1430A is V_{REF}. See Figure 34 for a further explanation of the common-mode voltage range for pseudo-differential inputs.

Figure 47. Pseudo-differential Input Mode of the RS1430A

The input current required by the analog inputs depends on a number of factors: sample rate, input voltage, source impedance, and power-down mode. Essentially, the current into the RS1430A charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (48pF) to a 16-bit settling level within 4.5 clock cycles (0.47μs). When the converter goes into Hold mode, or while it is in Power-Down mode, the input impedance is greater than 10MΩ.

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, the -IN input should not drop below GND-0.3V or exceed GND+0.5V. The +IN input should always remain within the range of GND-0.3V to VDD+0.3V, or -IN to -IN+VREF, whichever limit is reached first. Outside of these ranges, the converter linearity may not meet specifications. To minimize noise, low bandwidth input signals with low-pass filters should be used. In each case, care should be taken to ensure that the output impedance of the sources driving the +IN and –IN inputs are matched. Often, a small capacitor between the positive and negative inputs helps to match their impedance. To obtain maximum performance from the RS1430A, the input circuit from **Figure 48** is recommended.

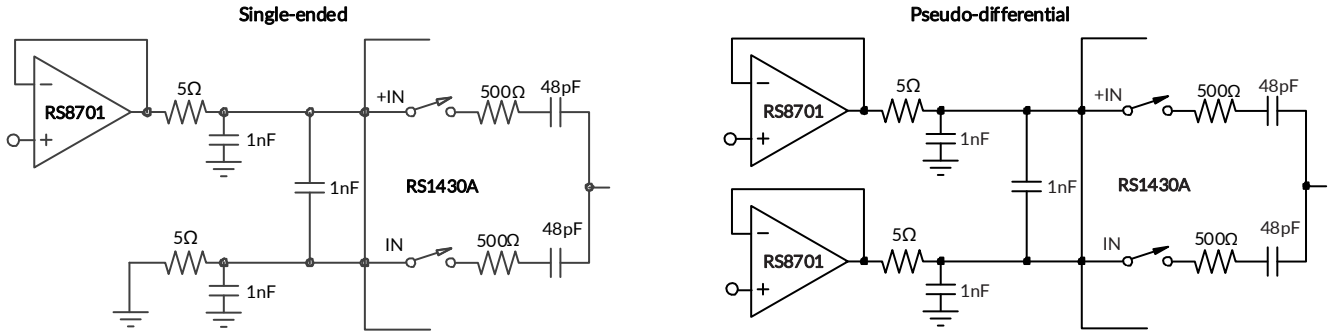


Figure 48. Single-ended and Pseudo-differential Methods of Interfacing the RS1430A

7.3 Reference Input

The external reference sets the analog input range. The RS1430A operates with a reference in the range of 0.1V to VDD. There are several important implications to this.

As the reference voltage is reduced, the analog voltage weight of each digital output code is reduced. This is often referred to as the least significant bit (LSB) size and is equal to the reference voltage divided by 65,536. This means that any offset or gain error inherent in the A/D converter will appear to increase (in terms of LSB size) as the reference voltage is reduced. For a reference voltage of 2.5V, the value of the LSB is 38.15μV, and for a reference voltage of 5V, the LSB is 76.3μV.

The noise inherent in the converter will also appear to increase with a lower LSB size. With a 5V reference, the internal noise of the converter typically contributes only 5LSB peak-to-peak of potential error to the output code. When the external reference is 2.5V, the potential error contribution from the internal noise will be two times larger (7LSB). The errors arising from the internal noise are Gaussian in nature and can be reduced by averaging consecutive conversion results.

With lower reference voltages, extra care should be taken to provide a clean layout including adequate bypassing, a clean power supply, a low-noise reference, and a low-noise input signal. Due to the lower LSB size, the converter is also more sensitive to external sources of error, such as nearby digital signals and electromagnetic interference.

The equivalent input circuit for the reference voltage is presented in **Figure 49**. During the conversion process, an equivalent capacitor of 48pF is switched on. To obtain optimum performance from the RS1430A, special care must be taken in designing the interface circuit to the reference input pin. To ensure a stable reference voltage, a 47μF tantalum capacitor with low ESR should be connected as close as possible to the input pin. If a high output impedance reference source is used, an additional operational amplifier with a current-limiting resistor must be placed in front of the capacitors.

When the RS1430A is in Power-Down mode, the input resistance of the reference pin will have a value of 10MΩ. Since the input capacitors must be recharged before the next conversion starts, an operational amplifier with good dynamic characteristics must be used to buffer the reference input.

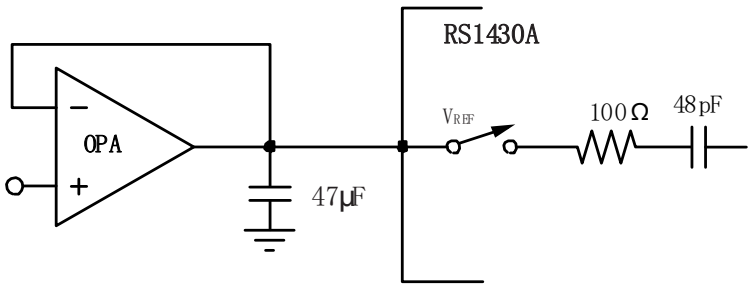


Figure 49. Input Reference Circuit and Interface

7.4 Noise

The transition noise of the RS1430A itself is extremely low, as shown in **Figure 22** (+5V) and **Figure 43** (+2.7V); it is much lower than competing A/D converters. These histograms were generated by applying a low-noise DC input and initiating 8192 conversions. The digital output of the A/D converter will vary in output code because of the internal noise of the RS1430A. Using a histogram to plot the output codes, the distribution should appear bell-shaped with the peak of the bell curve representing the nominal code for the input value. The ±1σ, ±2σ, and ±3σ distributions will represent 68.3%, 95.5%, and 99.7%, respectively, of all codes. The transition noise can be calculated by dividing the number of codes measured by 6, which yields the ±3σ distribution, or 99.7%, of all codes. Statistically, up to three codes could fall outside the distribution when executing 1000 conversions. The RS1430A, with < 5 output codes for the ±3σ distribution, yields < ±0.6LSB of transition noise. Remember, to achieve this low-noise performance, the peak-to-peak noise of the input signal and reference must be < 50μV.

7.5 Signal Levels

The RS1430A has a wide range of power-supply voltage. The A/D converter, as well as the digital interface circuit, is designed to accept and operate from 2.7V up to 5.5V. This voltage range will accommodate different logic levels. When the RS1430A power-supply voltage is in the range of 4.5V to 5.5V (5V logic level), the RS1430A can be connected directly to another 5V, CMOS integrated circuit. When the RS1430A power-supply voltage is in the range of 2.7V to 3.6V (3V logic level), the RS1430A can be connected directly to another 3.3V LVCMOS integrated circuit.

8 DIGITAL INTERFACE

8.1 Serial Interface

The RS1430A communicates with microprocessors and other digital systems via a synchronous 3-wire serial interface, as illustrated in the Timing Information section. The DCLOCK signal synchronizes the data transfer, with each bit being transmitted on the falling edge of DCLOCK. Most receiving systems will capture the bitstream on the rising edge of DCLOCK. However, if the minimum hold time for DOUT is acceptable, the system can use the falling edge of DCLOCK to capture each bit.

A falling CS signal initiates the conversion and data transfer. The first 4.5 to 5.0 clock periods of the conversion cycle are used to sample the input signal. After the fifth falling DCLOCK edge, DOUT is enabled and will output a low value for one clock period. For the next 16 DCLOCK periods, DOUT will output the current conversion result, most significant bit first. After the least significant bit (B0) has been output, subsequent clocks will repeat the output data, but in a least significant bit first format.

A new conversion is initiated only when CS has been taken high and returned low.

8.2 Data Format

The output data from the RS1430A is in Straight Binary format, as shown in **Figure 50**. This figure represents the ideal output code for a given input voltage and does not include the effects of offset, gain error, or noise.

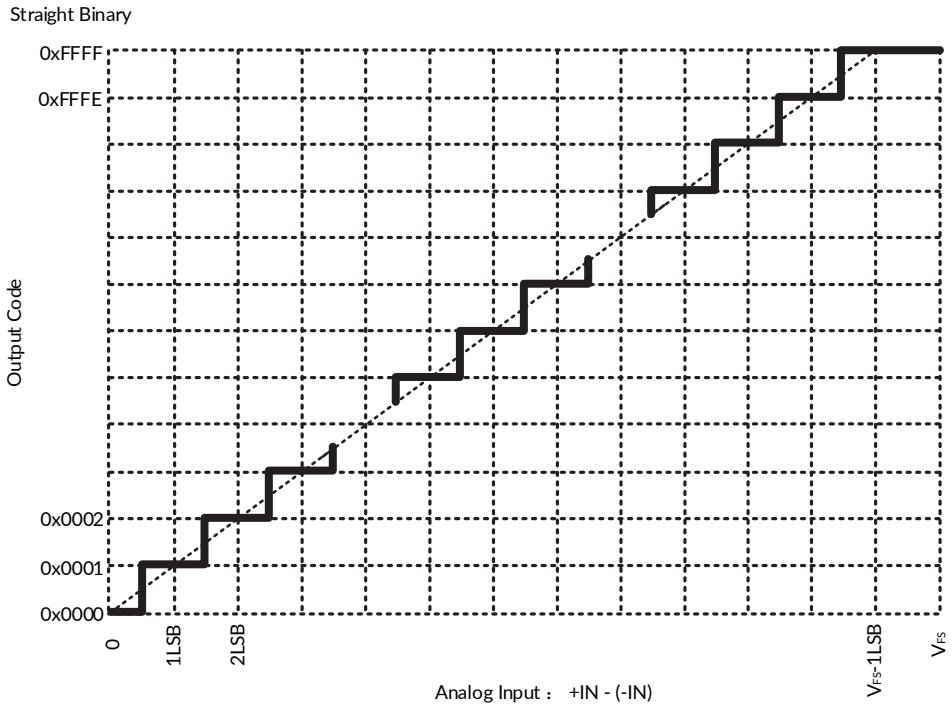


Figure 50. RS1430A Ideal Transfer Characteristic

9 POWER DISSIPATION

The power dissipation of the RS1430A scales directly with conversion rate. Therefore, the first step to achieving the lowest power dissipation is to find the lowest conversion rate that will satisfy the requirements of the system.

In addition, the RS1430A goes into Power-Down mode under two conditions: when the conversion is complete and whenever CS is high (see the Timing Information section). Ideally, each conversion should occur as quickly as possible, preferably at a 9.6MHz clock rate. This way, the converter spends the longest possible time in Power-Down mode. This is very important because the converter not only uses power on each DCLOCK transition (as is typical for digital CMOS components), but also uses some current for the analog circuitry, such as the comparator. The analog section dissipates power continuously until Power-Down mode is entered.

Figure 20 and **Figure 21** (+5V), and **Figure 41** and **Figure 42** (+2.7V) illustrate the current consumption of the RS1430A versus sample rate. For these graphs, the converter is clocked at maximum speed regardless of the sample rate. CS is held high during the remaining sample period.

There is an important distinction between the power-down mode that is entered after a conversion is complete and the full power-down mode that is enabled when CS is high. CS low will only shut down the analog section. The digital section is completely shut down only when CS is high. Thus, if CS is left low at the end of a conversion, and the converter is continually clocked, the power consumption will not be as low as when CS is high.

10 APPLICATION AND IMPLEMENTATION

Figure 51 and **Figure 52** show two examples of a basic data acquisition system. The 5Ω resistor and 0.1μF to 10μF capacitor filters the microcontroller noise on the supply, as well as any high-frequency noise from the supply itself. The exact values should be picked such that the filter provides adequate rejection of noise.

The 100Ω resistors serial on CS and DCLOCK are used to filter out the digital overshoot, respectively. The exact values should be selected based on the conversion speed, rising/falling time of CS and DCLOCK, and so on.

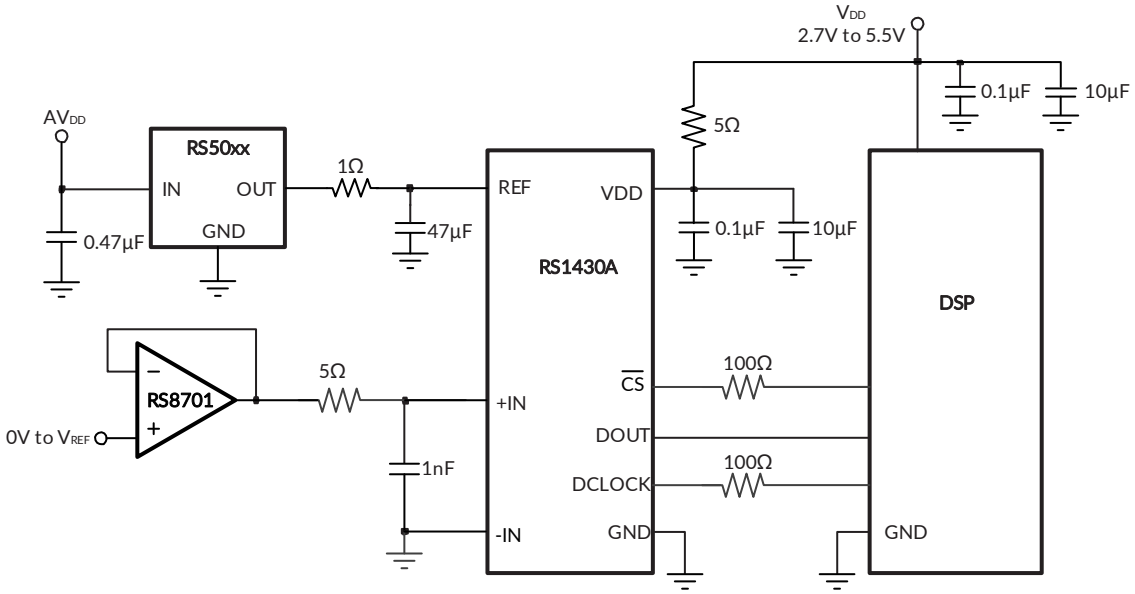


Figure 51. Basic Data Acquisition System: Example 1

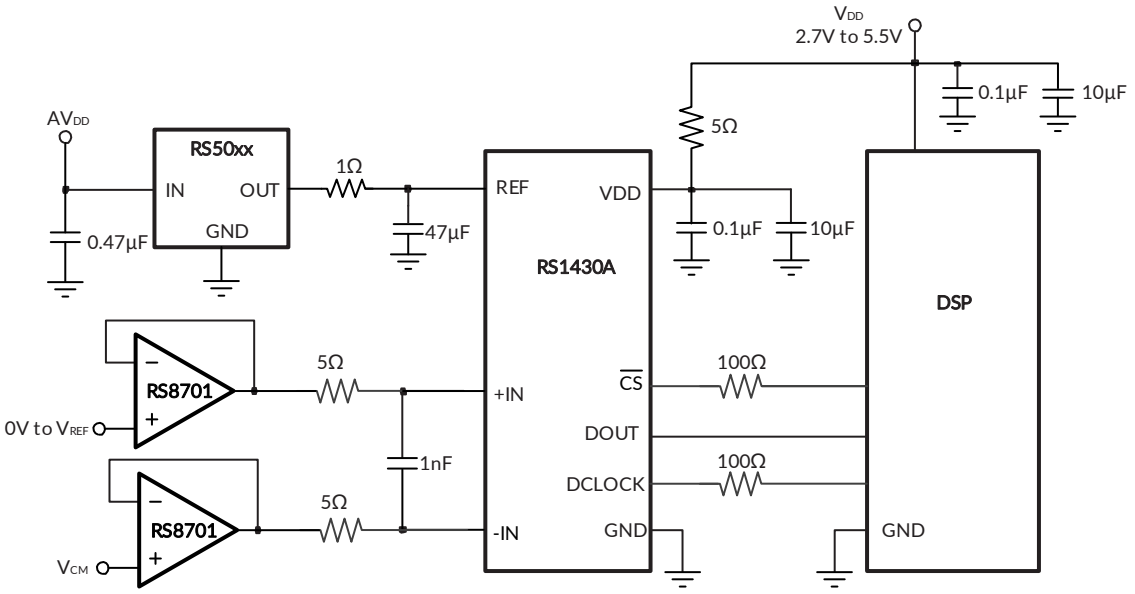
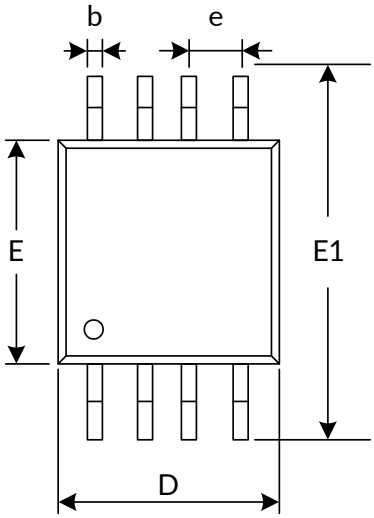
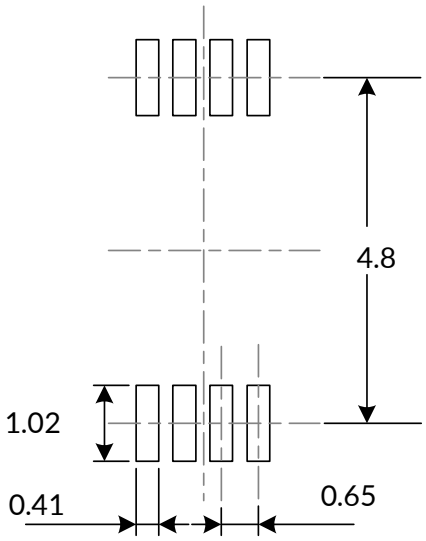


Figure 52. Basic Data Acquisition System: Example 2

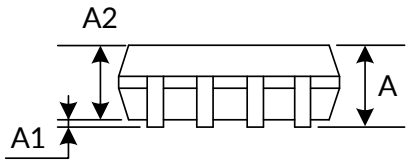
11 PACKAGE OUTLINE DIMENSIONS

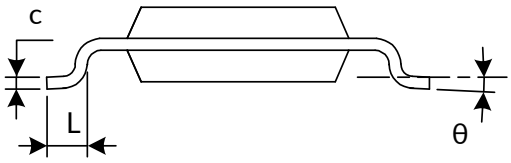
MSOP8 (3)





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D (1)	2.900	3.100	0.114	0.122
e	0.650(BSC) (2)		0.026(BSC) (2)	
E (1)	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

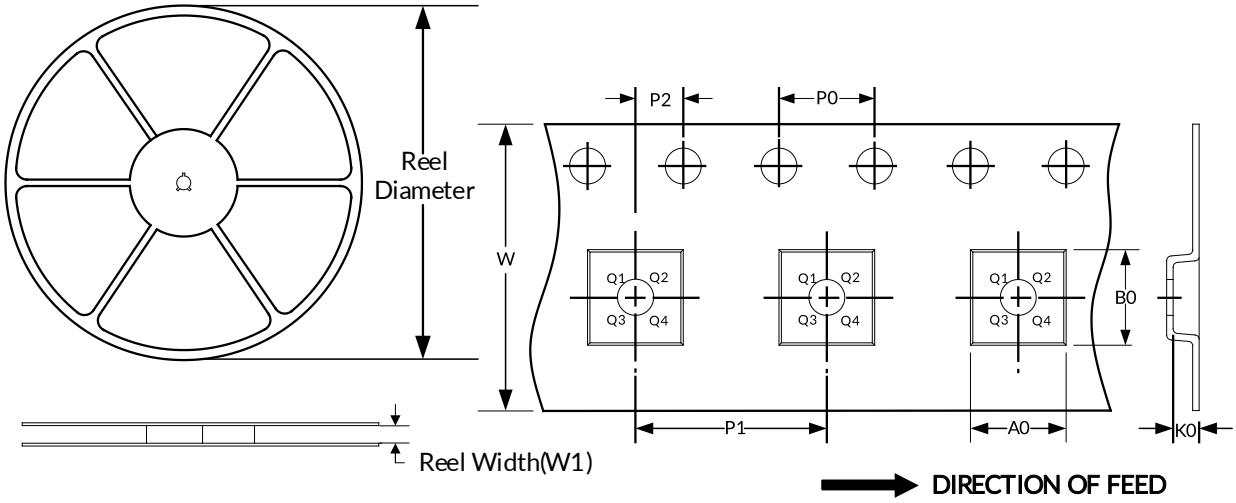
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

12 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
MSOP8	13”	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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