RS90LV049 3-V LVDS Dual Line Driver with Dual Line Receiver

1 FEATURES

- **Conforms to TIA/EIA-644 Standard**
- **＞400Mbps (200MHz) Switching Rates**
- **3.3V Power Supply**
- **±350mV Differential Signaling**
- **Supports Input Failsafe Open, Short, and Terminated**
- **Flow-Through Pinout Simplifies PCB Layout**
- **Low Power Dissipation (78mW at V_{DD}=3.3V Typical)**
- **TSSOP16 Package**
- **Industrial Temperature Operating Range (-40°C ~85°C)**

2 APPLICATIONS

- **Multifunction Printers**
- **LVDS-LVCMOS Translation**

3 ADVANTAGES

>200MHz Switching Rates.

Accept LVTTL/LVCMOS signals and small input swing (±350mV typically).

Support open, shorted, and terminated (100Ω) input fail-safe.

78mW low power dissipation.

TSSOP16 Package.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE(NOM)
RS90LV049	TSSOP16	5.00mm×4.40mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

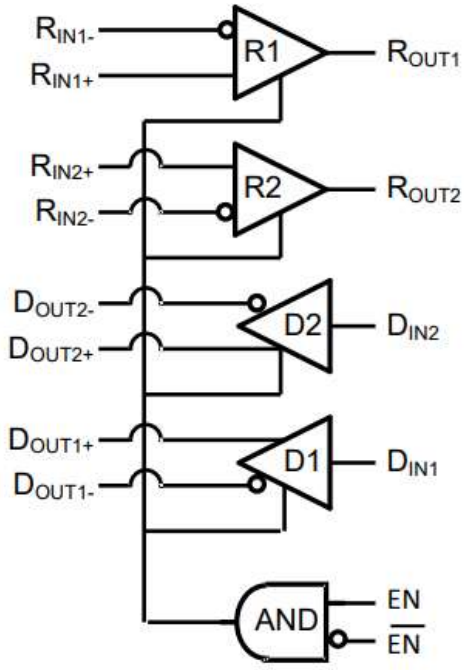


Figure 1. Functional Diagram

Table of Contents

1 FEATURES 1
2 APPLICATIONS 1
3 ADVANTAGES 1
4 REVISION HISTORY 3
5 PACKAGE/ORDERING INFORMATION (1) 4
6 DESCRIPTION 5
7 PIN CONFIGURATIONS 6
8 SPECIFICATIONS 7
8.1 Absolute Maximum Ratings 7
8.2 Recommended Operating Conditions 7
8.3 ESD Ratings 7
8.4 Electrical Characteristics 8
8.5 Switching Characteristics 9
9 TEST CIRCUITS AND TRANSITION TIME WAVEFORMS 10
10 PACKAGE OUTLINE DIMENSIONS 13
11 TAPE AND REEL INFORMATION 14

4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2024/11/12	Initial version
A.1	2024/12/16	Add machine test results

5 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	PACKAGE LEAD	TEMPERATURE RANGE	PACKAGE MARKING (2)	MSL (3)	PACKAGE OPTION
RS90LV049	RS90LV049YTSS16	TSSOP16	-40°C ~85°C	RS90LV049	MSL1	Tape and Reel, 4000

NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F, Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

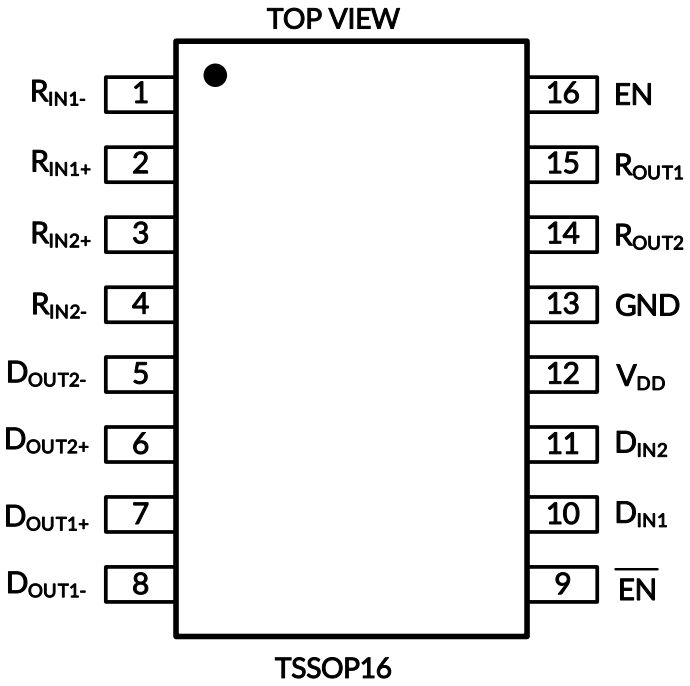
6 DESCRIPTION

The RS90LV049 is a dual CMOS flow-through differential line driver-receiver pair designed for applications requiring ultra low power dissipation, exceptional noise immunity, and high data throughput. The device is designed to support data rates in excess of 400 Mbps utilizing Low Voltage Differential Signaling (LVDS) technology.

The RS90LV049 drivers accept LVTTL/LVCMOS signals and translate them to LVDS signals. On the other hand, the receivers accept LVDS signals and translate them to 3 V CMOS signals. The LVDS input buffers have internal failsafe biasing that places the outputs to a known H (high) state for floating receiver inputs. In addition, the RS90LV049 supports a TRI- STATE function for a low idle power state when the device is not in use.

The EN and $\overline{EN}$ inputs are ANDed together and control the TRI-STATE outputs. The enables are common to all four gates.

7 PIN CONFIGURATIONS



PIN DESCRIPTION

Name	PIN	DESCRIPTION
EN	16	Enable pin: When EN is low, the driver/receiver is disabled. When EN is high and $\overline{EN}$ is low or open, the driver/receiver is enabled. If both EN and $\overline{EN}$ are open circuit, then the driver/receiver is disabled.
$\overline{EN}$	9	Disable pin: When $\overline{EN}$ is high, the driver/receiver is disabled. When $\overline{EN}$ is low or open and EN is high, the driver/receiver is enabled. If both EN and $\overline{EN}$ are open circuit, then the driver/receiver is disabled.
GND	13	Ground pin
R_{IN+}	2,3	Non-inverting receiver input pins
R_{IN-}	1,4	inverting receiver input pins
R_{OUT}	14,15	Receiver output pins
D_{IN}	10,11	Driver input pins
D_{OUT+}	6,7	Non-inverting driver output pins
D_{OUT-}	5,8	Inverting driver output pins
V_{DD}	12	Power supply pin, 3.3 V ± 0.3 V

8 SPECIFICATIONS

8.1 Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Supply Voltage (V_{DD})	-0.3	4	V
LVCMOS Input Voltage (D_{IN})	-0.3	V_{DD}+0.3	V
LVDS Input Voltage (R_{IN+}, R_{IN-})	-0.3	3.9	V
Enable Input Voltage (EN, $\overline{EN}$)	-0.3	V_{DD}+0.3	V
LVCMOS Output Voltage (R_{OUT})	-0.3	V_{DD}+0.3	V
LVDS Output Voltage (D_{OUT+}, D_{OUT-})	-0.3	3.9	V
LVCMOS Output Short Circuit Current (R_{OUT})		100	mA
LVDS Output Short Circuit Current Duration (D_{OUT+}, D_{OUT-})		24	mA
Maximum Junction Temperature		150	°C
Storage Temperature Range	-65	150	°C

Note: Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be specified. They are not meant to imply that the devices should be operated at these limits.

8.2 Recommended Operating Conditions

	MIN	TYP	MAX	UNIT
Supply Voltage (V_{DD})	3	3.3	3.6	V
Temperature (T_A)	-40	25	85	°C

8.3 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

		VALUE	UNIT
$V_{(ESD)}$	Human-Body Model (HBM)	≥8000	V
	Charged-Device Model (CDM)	≥2000	V
	Latch-Up (LU)	≥400	mA

Electric devices and circuit boards may discharge undetected. Although this product has a patented or proprietary protection circuit, the device may be damaged when exposed to high energy ESD. Therefore, appropriate ESD prevention measures should be taken to avoid device performance degradation or loss of function.

8.4 Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. V_{DD}=+3.3V±10%，T_A= -40°C to 85°C.

SYMBOL	PARAMETER	CONDITIONS	PIN	MIN	TYP	MAX	UNIT
LVCMOS Input DC Specifications (Driver Inputs, ENABLE Pins)							
V_{IH}	Input High Voltage		D_{IN} EN $\overline{EN}$	2		V_{DD}	V
V_{IL}	Input Low Voltage			GND		0.8	V
I_{IH}	Input High Current	$V_{IN}=V_{DD}$		-10	5	+10	μA
I_{IL}	Input Low Current	V_{IN}=GND		-10	0	+10	μA
LVDS Output DC Specifications (Driver Outputs)							
$\|V_{OD}\|$	Differential Output Voltage	R_L=100Ω (Figure 2)	D_{OUT-} D_{OUT+}	250	350	450	mV
V_{OS}	Offset Voltage			1.125	1.22	1.375	V
I_{OS}	Output Short Circuit Current	ENABLED, $D_{IN}=V_{DD}$, D_{OUT+}=0V or D_{IN}=GND, D_{OUT-}=0V			-7.85	-9	mA
I_{OSD}	Differential Output Short Circuit Current	ENABLED, V_{OD}=0			-4.4	-9	mA
I_{OFF}	Power-off Leakage	V_{OUT}=0 or 3.6V, V_{DD}=0V or open		-20	±1	+20	μA
I_{OZ}	Output TRI-STATE Current	EN=0V and $\overline{EN}=V_{DD}$ V_{OUT}=0V or V_{DD}		-10	±1	+10	μA
LVDS Input DC Specifications (Receiver Inputs)							
V_{TH}	Differential Input High Threshold	V_{CM}=1.2V, 0.05V, 2.35V	R_{IN+} R_{IN-}		-15	35	mV
V_{TL}	Differential Input High Threshold			-100	-15		mV
V_{CMR}	Common-Mode Voltage Range	V_{DD}=3.3V, V_{ID}=100mV		0.05		3	V
I_{IN}	Input Current	V_{DD}=3.6V, V_{IN}= 0V or 2.8V		-12	±4.2	+12	μA
		V_{DD}= 0V, V_{IN}= 0V or 2.8Vor 3.6V		-10	±1	+10	μA
LVCMOS Output DC Specifications (Receiver Outputs)							
V_{OH}	Output High Voltage	I_{OH}=-0.4mA, V_{ID}=+200mV	R_{OUT}	2.7	3.3		V
V_{OL}	Output Low Voltage	I_{OH}=2mA, V_{ID}=-200mV			0.06	0.25	V
I_{OZ}	Output TRI-STATE Current	Disabled, V_{OUT}=0 or V_{DD}		-10	±1	+10	μA
General DC Specifications							
I_{DD}	Power Supply Current	EN=3.3V	V_{DD}		23.6	35	mA
I_{DDZ}	TRI-State Supply Current	EN=0V			16.6	25	mA

Note:

1.Current into device pins is defined as positive. Current out of device pins is defined as negative.

2.All typical values are given for: V_{DD}=3.3V and T_A=25°C.

8.5 Switching Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
LVDS Outputs (Driver outputs)						
t_{PHLD}	Differential Propagation Delay High to Low	R_L=100Ω (Figure3 and Figure4)		1	2	ns
t_{PLHD}	Differential Propagation Delay Low to High			1.2	2	ns
t_{SKD1}	$\lvert t_{PHLD} - t_{PLHD} \rvert$		0.05	0.2	0.5	ns
t_{TLH}	Rise Time		0.5	0.65	1	ns
t_{THL}	Fall Time		0.5	0.65	1	ns
t_{PHZ}	Disable Time High to Z	R_L=100Ω (Figure5 and Figure6)		1.6	3	ns
t_{PLZ}	Disable Time Low to Z			1.8	3	ns
t_{PZH}	Enable Time Z to High		1.4	3.4	6	ns
t_{PZL}	Enable Time Z to Low		1.2	2	6	ns
f_{MAX}	Maximum Operating Frequency		200	250		MHz
LVCMOS Outputs (Receiver Outputs)						
t_{PHL}	Propagation Delay High to Low	(Figure7 and Figure8)	1.3	2.7	3.5	ns
t_{PLH}	Propagation Delay Low to High		1.3	2.7	3.5	ns
t_{SKD1}	$\lvert t_{PHLD} - t_{PLHD} \rvert$			0.3	0.4	ns
t_{TLH}	Rise Time		0.5	0.9	1.4	ns
t_{THL}	Fall Time		0.5	0.7	1.4	ns
t_{PHZ}	Disable Time High to Z	(Figure9 and Figure10)	4.5	5.6	8	ns
t_{PLZ}	Disable Time Low to Z		4.2	5.4	8	ns
t_{PZH}	Enable Time Z to High		2	2.6	7	ns
t_{PZL}	Enable Time Z to Low		2	2.6	7	ns
f_{MAX}	Maximum Operating Frequency		200	250		MHz

Note:

1. Generator waveform for all tests unless otherwise specified: f=1MHz，Zo=50Ω，t_r≤1ns，t_f≤1ns.
2. f_{MAX} generator input conditions: $t_r = t_f$ < 1 ns (0% to 100%), 50% duty cycle, 0 V to 3 V. Output Criteria: duty cycle = 45%/55%, V_{OD} > 250 mV, all channels switching.
3. f_{MAX} generator input conditions: $t_r = t_f$ <1 ns (0%-100%), 50% duty cycle, differential (1.05-V to 1.35-V peak to peak). Output criteria: 45%/55% duty cycle, V_{OL} (maximum 0.25 V), V_{OH} (minimum 2.7 V).

9 TEST CIRCUITS AND TRANSITION TIME WAVEFORMS

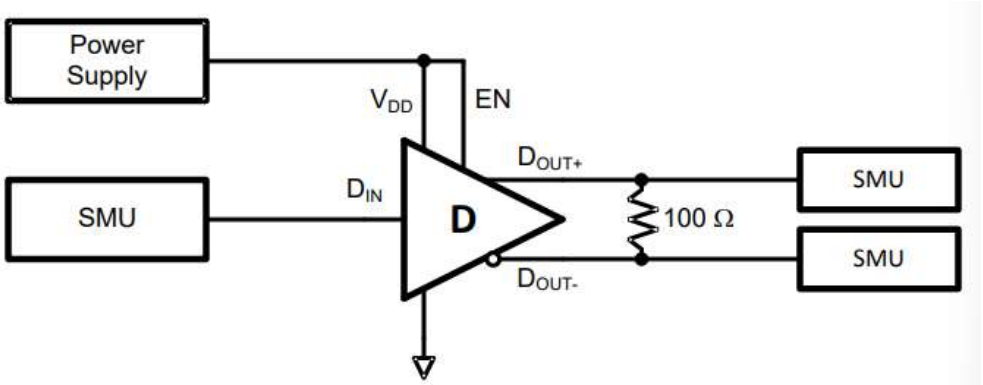


Figure 2. Driver V_{OD} and V_{OS} Test Circuit

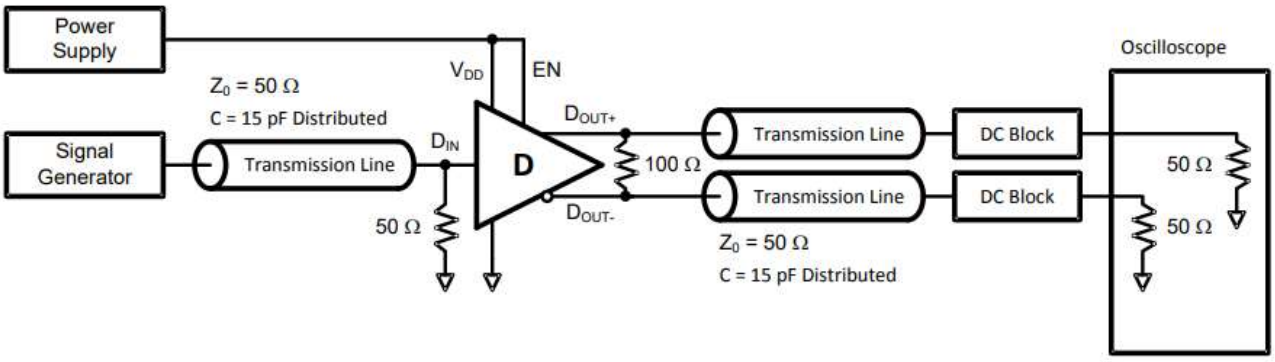


Figure 3. Driver Propagation Delay and Transition Time Test Circuit

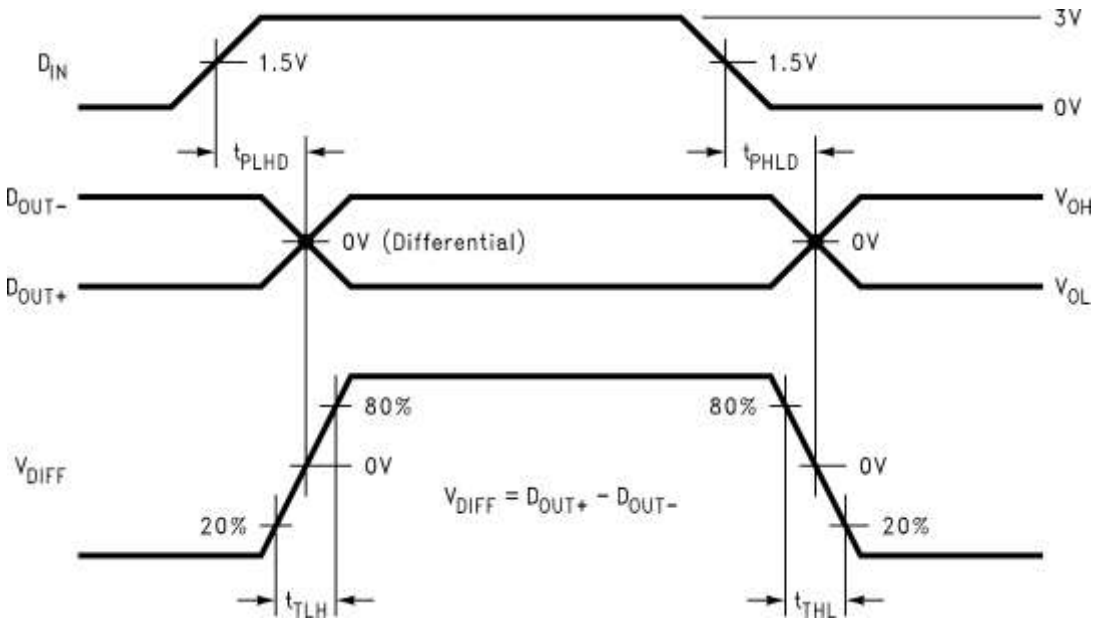


Figure 4. Driver Propagation Delay and Transition Time Waveforms

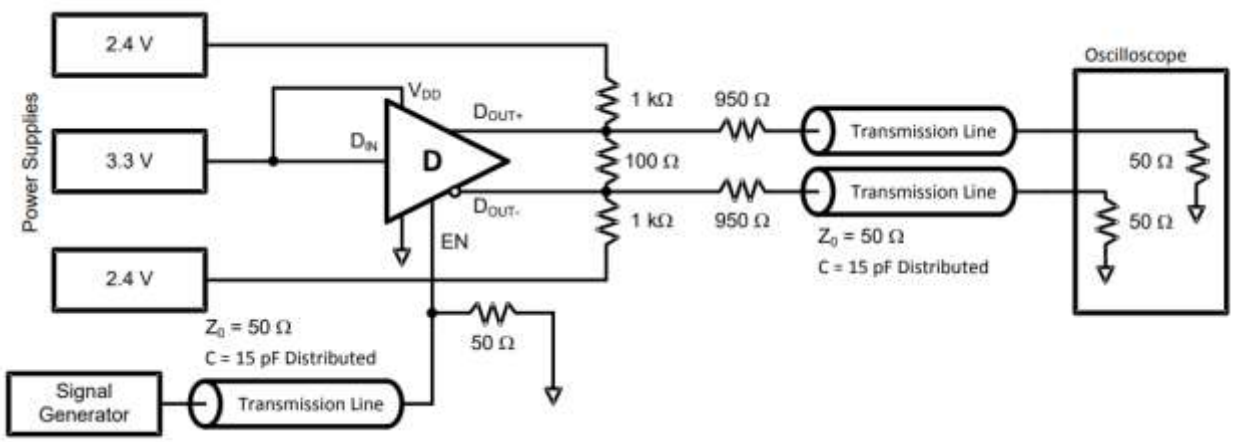


Figure 5. Driver TRI-STATE Delay Test Circuit

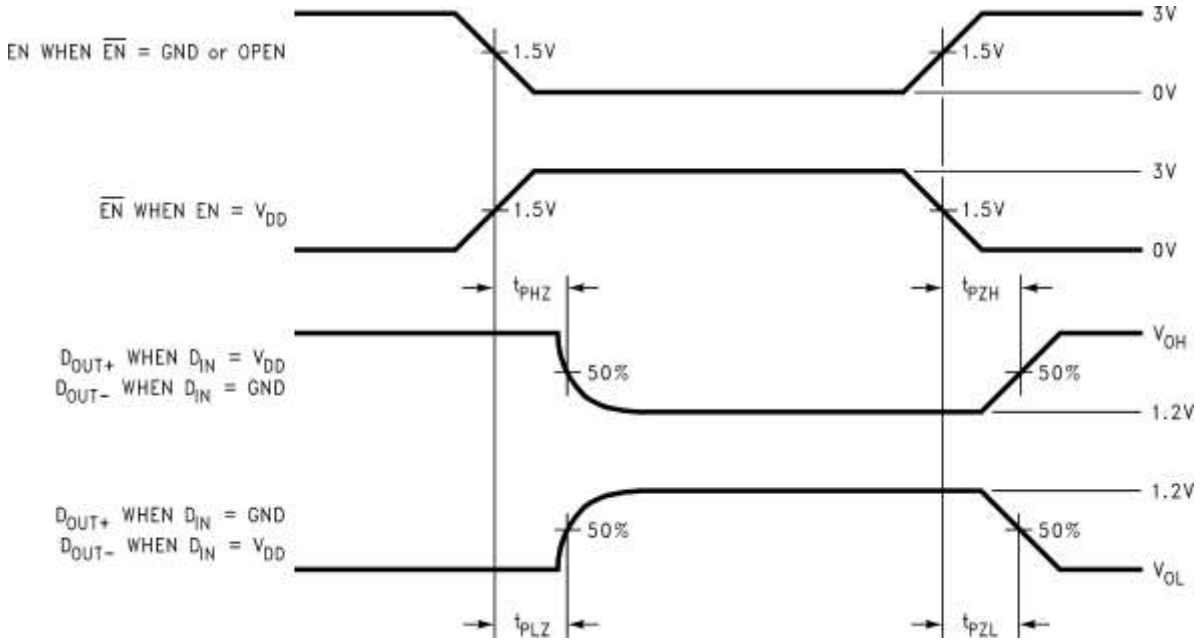


Figure 6. Driver TRI-STATE Delay Waveforms

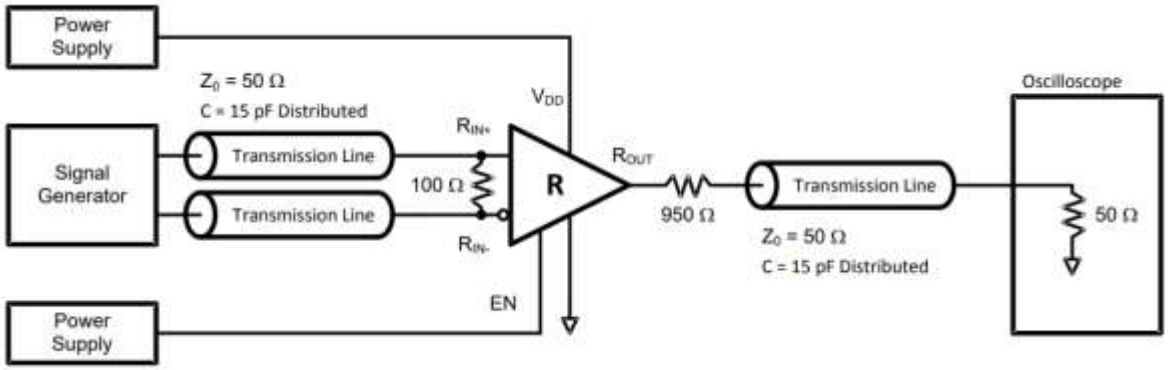


Figure 7. Receiver Propagation Delay and Transition Time Test Circuit

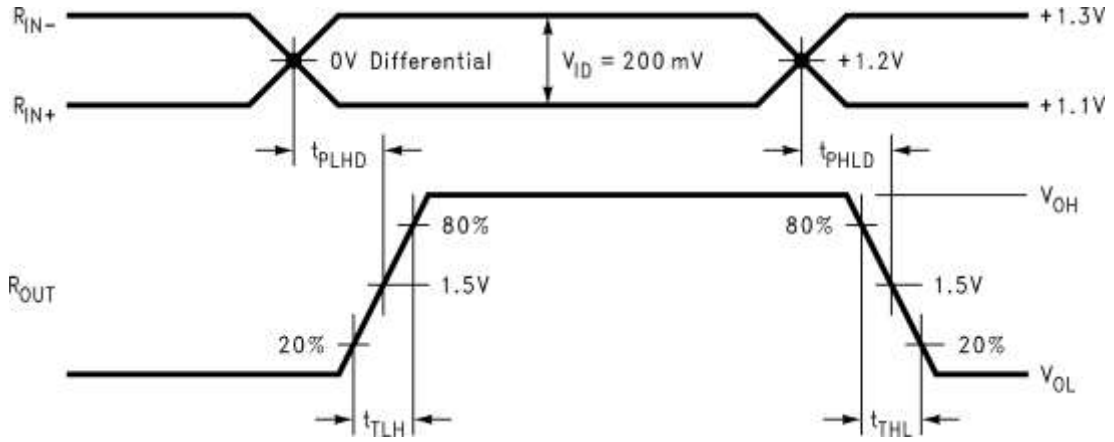


Figure 8. Receiver Propagation Delay and Transition Time Waveforms

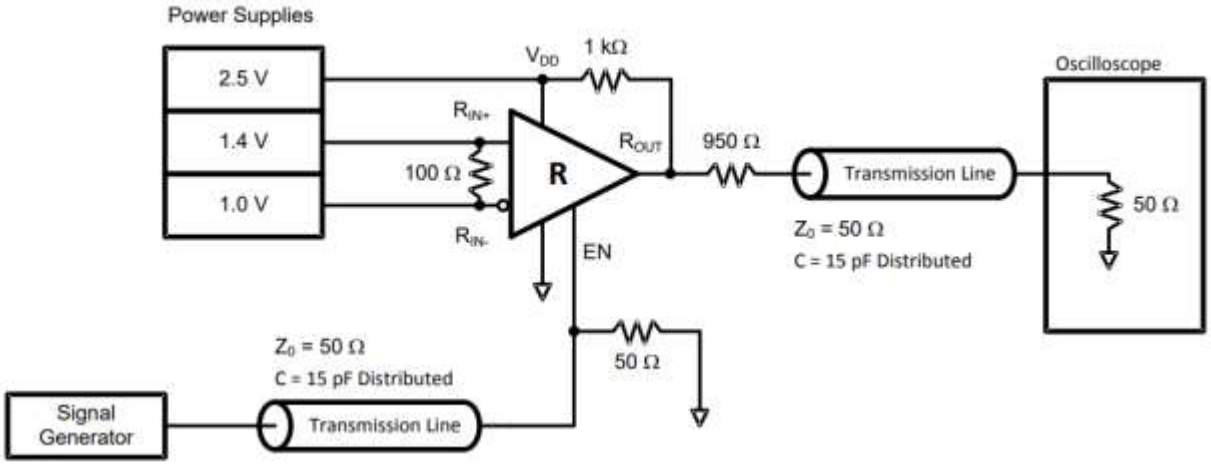


Figure 9. Receiver TRI-STATE Delay Test Circuit

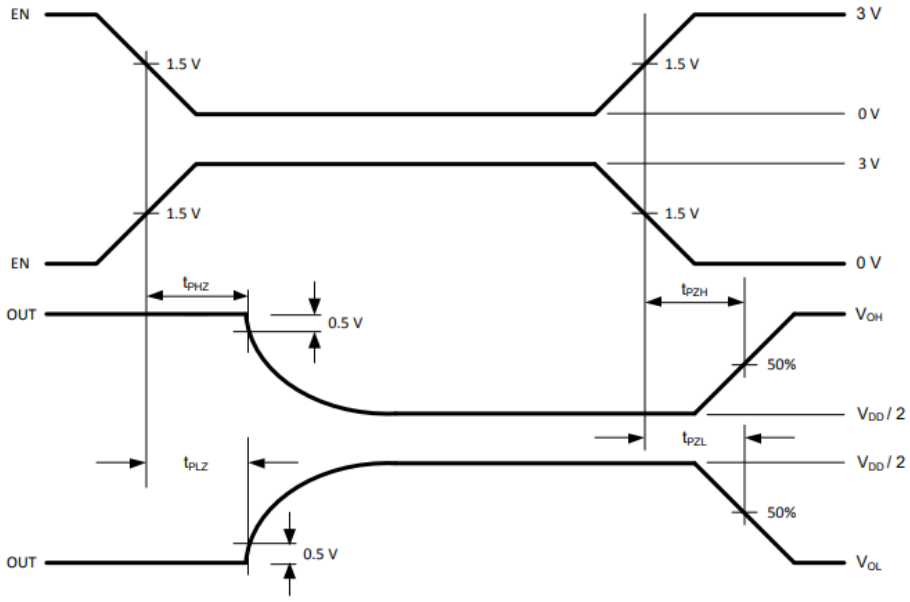
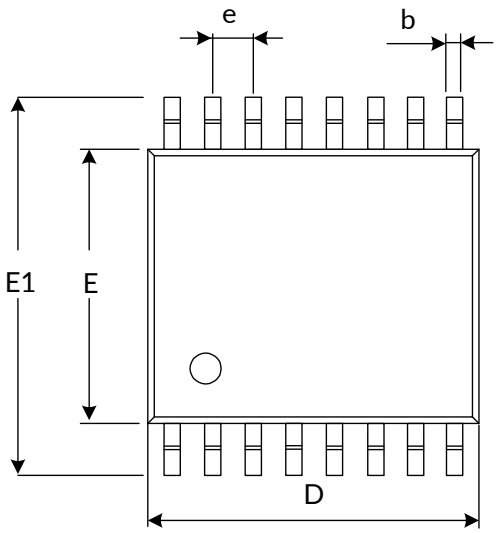
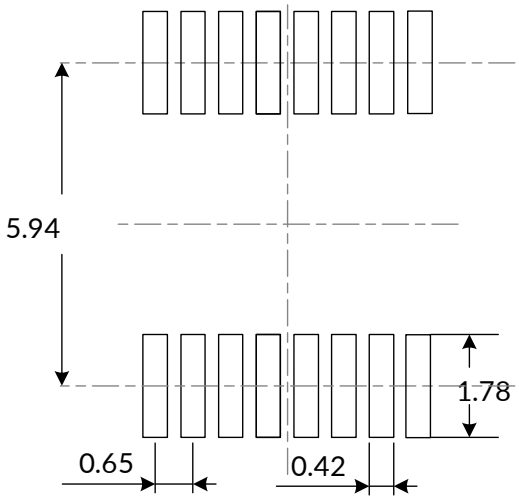


Figure 10. Receiver TRI-STATE Delay Waveforms

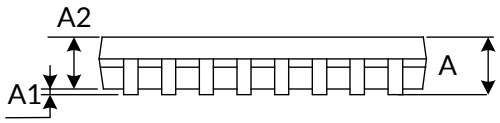
10 PACKAGE OUTLINE DIMENSIONS

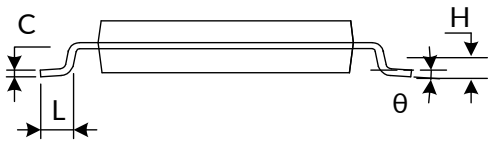
TSSOP16 (3)





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D (1)	4.860	5.100	0.191	0.201
E (1)	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.244	0.260
e	0.650(BSC) (2)		0.026(BSC) (2)	
L	0.500	0.700	0.02	0.028
H	0.250 TYP		0.010 TYP	
θ	1°	7°	1°	7°

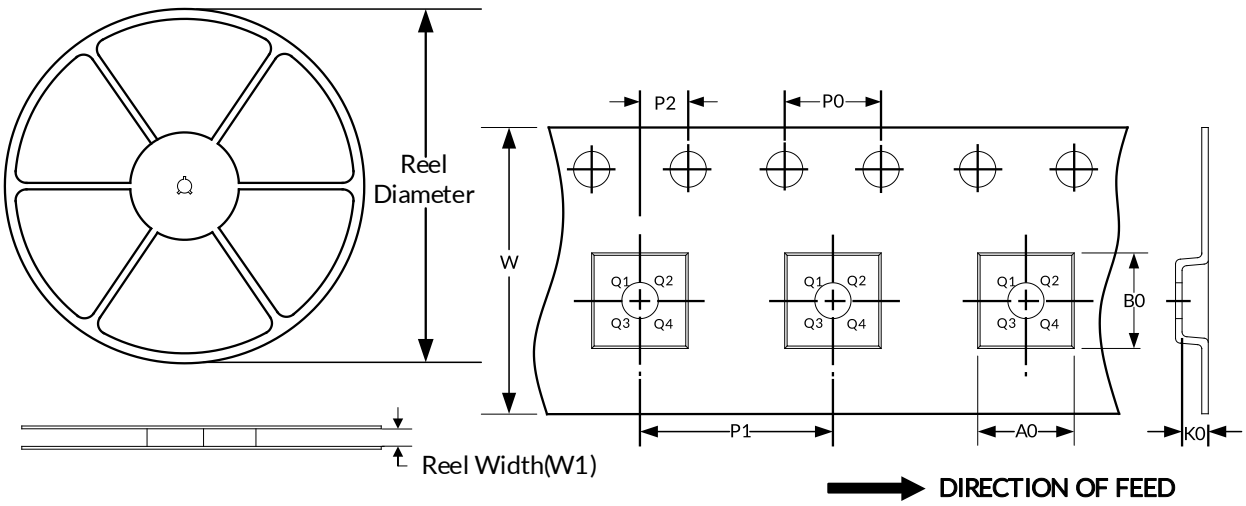
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

11 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP16	13”	12.4	6.90	5.60	1.20	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

IMPORTANT NOTICE AND DISCLAIMER

Jiangsu RUNIC Technology Co., Ltd. will accurately and reliably provide technical and reliability data (including data sheets), design resources (including reference designs), application or other design advice, WEB tools, safety information and other resources, without warranty of any defect, and will not make any express or implied warranty, including but not limited to the warranty of merchantability Implied warranty that it is suitable for a specific purpose or does not infringe the intellectual property rights of any third party.

These resources are intended for skilled developers designing with RUNIC products You will be solely responsible for: (1) Selecting the appropriate products for your application; (2) Designing, validating and testing your application; (3) Ensuring your application meets applicable standards and any other safety, security or other requirements; (4) RUNIC and the RUNIC logo are registered trademarks of RUNIC INCORPORATED. All trademarks are the property of their respective owners; (5) For change details, review the revision history included in any revised document. The resources are subject to change without notice. Our company will not be liable for the use of this product and the infringement of patents or third-party intellectual property rights due to its use.