36V Rail-to-Rail Input/Output, Low Offset Voltage, Low Noise Operational Amplifiers

1 FEATURES

- **Low Offset Voltage: ±0.2mV (TYP)**
- **Low Offset Voltage Drift: ±1μV/°C**
- **Low Noise: 5.5μV$_{PP}$ (0.1Hz ~ 10Hz)**
- **High Common-Mode Rejection: 120dB**
- **Rail-to-Rail Input and Output**
- **Wide Bandwidth: 5MHz**
- **High Slew Rate: 23V/μs**
- **High Capacitive Load Drive: 100pF**
- **MUX-Friendly/Comparator Inputs**
  - **Amplifier Operates with Differential Inputs up to Supply Rail**
  - **Amplifier Can Be used in Open-Loop or as Comparator**
- **Low Quiescent Current: 500μA Per Amplifier**
- **Wide Supply: ±2V to ±18V, 4V to 36V**
- **Robust EMIRR Performance: EMI/RFI Filters on Input and Supply Pins**
- **Differential and Common-Mode Input Voltage Range to Supply Rail**

2 APPLICATIONS

- **Low-Power Audio Preamplifier**
- **Multiplexed Data-Acquisition Systems**
- **Test and Measurement Equipment**
- **ADC Driver Amplifiers**
- **SAR ADC Reference Buffers**
- **Programmable Logic Controllers**
- **High-Side and Low-Side Current Sensing**

3 DESCRIPTIONS

The RS8447, RS8448 is a family of high voltage (36V) general purpose operational amplifiers. These devices offer exceptional DC precision and AC performance, including rail-to-rail input/output, low offset (±0.2mV, typical), low offset drift (±1μV/°C, typical), low noise (5.5μV$_{PP}$), and 5MHz bandwidth.

Unique features such as differential and common mode input-voltage range to the supply rail, high output current (70mA), high slew rate (23V/μs), high capacitive load drive (100pF), and shutdown functionality make the RS8447, RS8448 a robust, high performance operational amplifier for high-voltage industrial applications.

The RS8447/RS8448 are specified for the extended industrial and automotive temperature range (-40°C to 125°C). The RS8447 single amplifier is available in SOT23-5. The RS8448 dual amplifier is available in SOP8 and MSOP8 packages.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE(NOM)
RS8447	SOT23-5	2.90mm×1.60mm
RS8448	SOP8	4.90mm×3.90mm
	MSOP8	3.00mm×3.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Table of Contents

4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

Version	Change Date	Change Item
A.0	2025/01/03	Preliminary version completed
A.1	2025/05/23	Initial version completed

5 PACKAGE/ORDERING INFORMATION (1)

Orderable Device	Package Type	Pin	Channel	Op Temp (°C)	Device Marking (2)	MSL (3)	Package Qty
RS8447XF	SOT23-5	5	1	-40°C ~ 125°C	8447	MSL1	Tape and Reel, 3000
RS8448XK	SOP8	8	2	-40°C ~125°C	RS8448	MSL1	Tape and Reel, 4000
RS8448XM	MSOP8	8	2	-40°C ~125°C	RS8448	MSL1	Tape and Reel, 4000

NOTE:

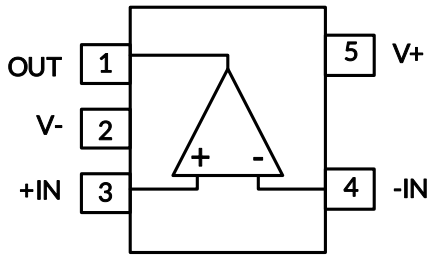
(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

6 PIN CONFIGURATION AND FUNCTIONS

RS8447



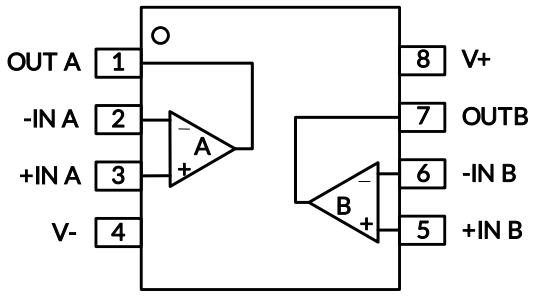
SOT23-5

PIN DESCRIPTION

NAME	PIN	I/O (1)	DESCRIPTION
	SOT23-5		
-IN	4	I	Negative (inverting) input
+IN	3	I	Positive (noninverting) input
OUT	1	O	Output
V-	2	-	Negative (lowest) power supply
V+	5	-	Positive (highest) power supply

(1) I = Input, O = Output.

RS8448



SOP8/MSOP8

PIN DESCRIPTION

NAME	PIN	I/O (1)	DESCRIPTION
	SOP8/MSOP8		
-INA	2	I	Inverting input, channel A
+INA	3	I	Noninverting input, channel A
-INB	6	I	Inverting input, channel B
+INB	5	I	Noninverting input, channel B
OUTA	1	O	Output, channel A
OUTB	7	O	Output, channel B
V-	4	-	Negative (lowest) power supply
V+	8	-	Positive (highest) power supply

(1) I = Input, O = Output.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Voltage	Supply, V_S= (V+) - (V-)		0	42	V
	Signal input pin (2)		(V-) - 0.5	(V+) + 0.5	
	Signal output pin (3)		(V-) - 0.5	(V+) + 0.5	
	Differential input voltage		(V-) - (V+)	(V+) - (V-)	
Current	Signal input pin (2)		-10	10	mA
	Signal output pin (3)		-50	50	mA
	Output short-circuit (4)		Continuous		
θ_{JA}	Package thermal impedance (5)	SOT23-5		230	°C/W
		SOP8		110	
		MSOP8		170	
Temperature	Operating range, T_A		-40	125	°C
	Junction, T_J (6)			150	
	Storage, T_{stg}		-65	150	

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.
(3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.5V beyond the supply rails should be current-limited to ±50mA or less.
(4) Short-circuit to ground, one amplifier per package.
(5) The package thermal impedance is calculated in accordance with JESD-51.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), ANSI/ESDA/JEDEC JS001-2023	±2000	V
		Charged-Device Model (CDM), ANSI/ESDA/JEDEC JS-002-2022	±1500	

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, V_S= (V+) - (V-)	Single-supply	4		36	V
	Dual-supply	±2		±18	

7.4 Electrical Characteristics

(At T_A= +25°C, V_S= 36V, R_L= 10kΩ, T_A [9] = -40°C to 125°C, unless otherwise noted.) [1]

PARAMETER		CONDITIONS	T_A	RS8447, RS8448			UNIT
				MIN[2]	TYP[3]	MAX[2]	
POWER SUPPLY							
V_S	Operating Voltage Range		Full	4		36	V
I_Q	Quiescent Current per Amplifier	V_S=±2.5V, I_O=0mA	25°C		500	700	μA
			Full			800	
		V_S=±18V, I_O=0mA	25°C		550	750	
			Full			850	
PSRR	Power-Supply Rejection Ratio	V_S=4V to 36V	25°C	100	115		dB
			Full	90			
INPUT							
Vos	Input Offset Voltage	V_S=5V, V_{CM}=2.5V	25°C	-1	±0.2	1	mV
			Full	-2		2	
		V_S=36V, V_{CM}=18V	25°C	-1	±0.2	1	mV
			Full	-2		2	
Vos Tc	Input Offset Voltage Drift		Full		±1		μV/°C
IB	Input Bias Current [4] [5]	V_S=36V, V_{CM}=18V	25°C		±20		pA
I_{OS}	Input Offset Current [4]	V_S=36V, V_{CM}=18V	25°C		±20		pA
A_{OL}	Open-loop Voltage Gain	R_{LOAD}=10kΩ, V_{OUT}=0.1 V to 35.9 V	25°C	115	130		dB
			Full	110			dB
V_{CM}	Common-Mode Voltage Range		Full	(V-)-0.1		(V+)+0.1	V
CMRR	Common-Mode Rejection Ratio	V_S=36V, V−< V_{CM} < (V+)−2.5V (PMOS pair)	25°C	105	120		dB
			Full	100			
		V_S=5V, V−< V_{CM} < (V+)−2.5V (PMOS pair)	25°C	85	100		
			Full	80			
		V_S=3V to 36V, (V+)−1V < V_{CM} < V+ (NMOS pair)	25°C	65	85		
		(V+)−2.5V < V_{CM} < (V+)−1V	Full	See Offset Voltage vs Common-Mode Voltage (Transition Region)			
OUTPUT							
V_{OH}	Output Swing from Positive Rail	V_S=36V, R_{LOAD}=10kΩ to V_S/2	25°C		40	180	mV
V_{OL}	Output Swing from Negative Rail	V_S=36V, R_{LOAD}=10kΩ to V_S/2	25°C		35	180	mV
I_{SC}	Short-Circuit Current [6] [7]	Source	25°C	35	65		mA
		Sink	25°C	45	70		
AC Specifications							
SR	Slew Rate [8]	G=1, V_{IN}=20V Step	25°C		23		V/μs
GBW	Gain-Bandwidth Product	G=11, V_{IN}=50mV, V_S=5V	25°C		5		MHz
t_s	Settling Time, 0.1%	G=1, V_{IN}=2V Step	25°C		10		μs
t_{OR}	Overload Recovery Time	V_{IN} · Gain ≥ V_S, G=11	25°C		600		ns
PM	Phase Margin [4]	R_L=10kΩ, C_L=50pF	25°C		66		°
GM	Gain Margin [4]	R_L=10kΩ, C_L=50pF	25°C		14		dB
C_{LOAD}	Capacitive Load Drive		25°C		100		pF

NOISE							
En	Input Voltage Noise	V_S=5V, f=0.1Hz to 10Hz	25°C		5.5		μVpp
en	Input Voltage Noise Density (4)	f=1kHz	25°C		22		nV/$\sqrt{Hz}$
		f=10kHz	25°C		16		

NOTE:
(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(4) This parameter is ensured by design and/or characterization and is not tested in production.
(5) Positive current corresponds to current flowing into the device.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.
(7) Short circuit test is a momentary test.
(8) Number specified is the slower of positive and negative slew rates.
(9) Specified by characterization only.

7.5 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = +25°C, V_S = ±18V, V_{CM} = 0V, R_L = 10kΩ, unless otherwise specified.

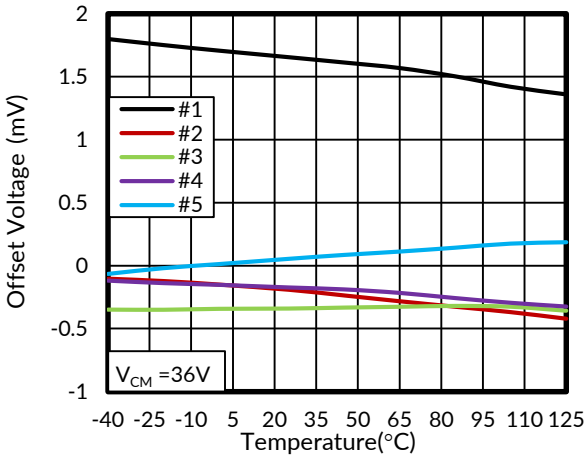


Figure 1. Offset Voltage vs Temperature

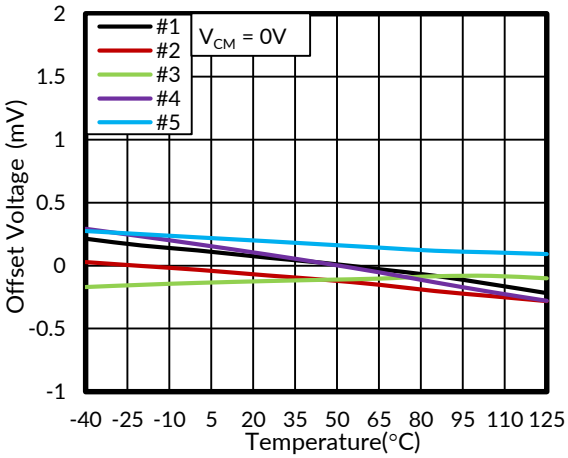


Figure 2. Offset Voltage vs Temperature

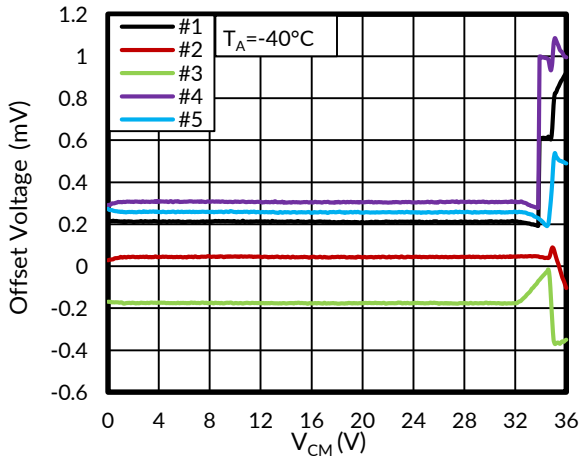


Figure 3. Offset Voltage vs Common Mode Voltage

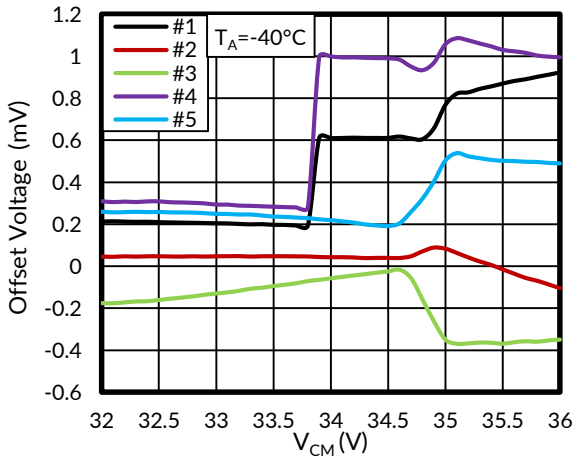


Figure 4. Offset Voltage vs Common Mode Voltage (Transition Region)

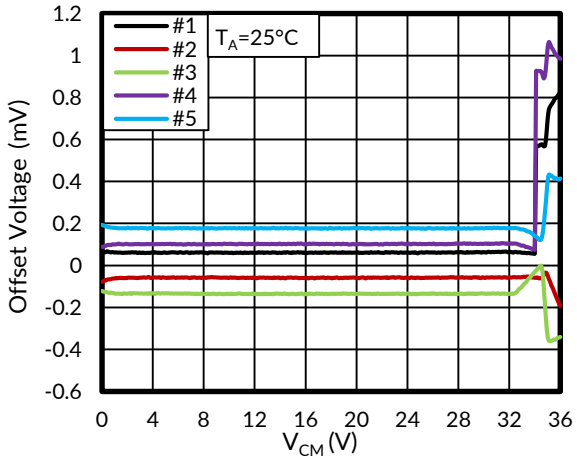


Figure 5. Offset Voltage vs Common Mode Voltage

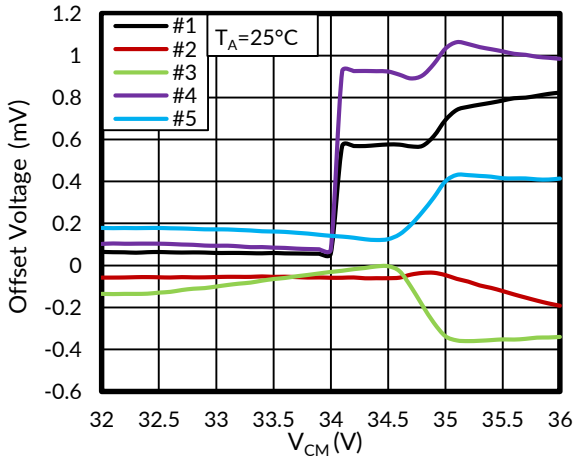


Figure 6. Offset Voltage vs Common Mode Voltage (Transition Region)

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = +25°C, V_S = ±18V, V_{CM} = 0V, R_L = 10kΩ, unless otherwise specified.

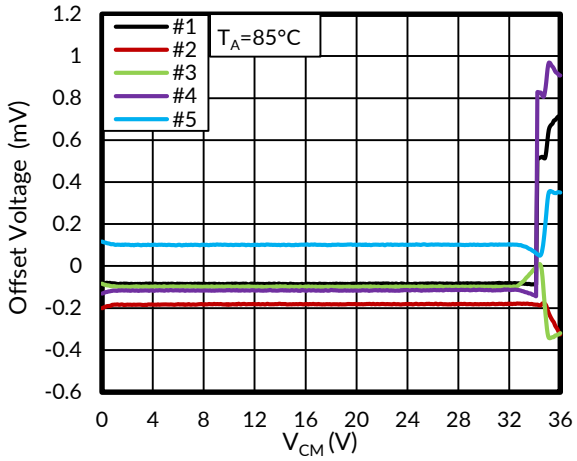


Figure 7. Offset Voltage vs Common Mode Voltage

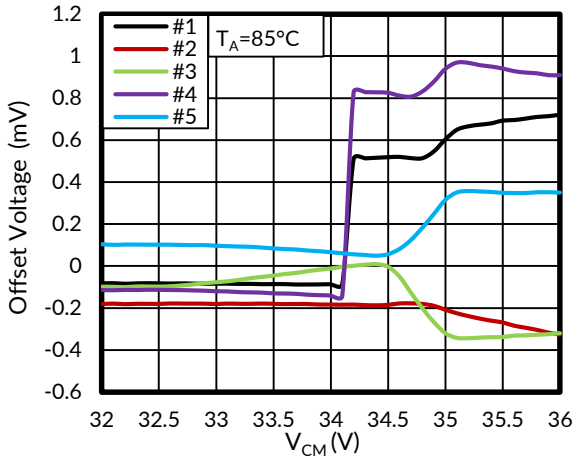


Figure 8. Offset Voltage vs Common Mode Voltage (Transition Region)

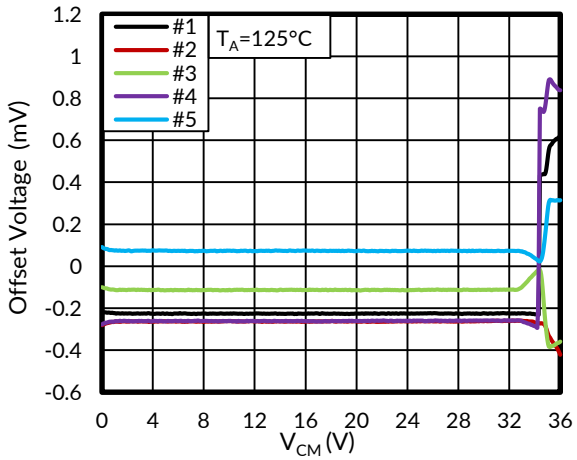


Figure 9. Offset Voltage vs Common Mode Voltage

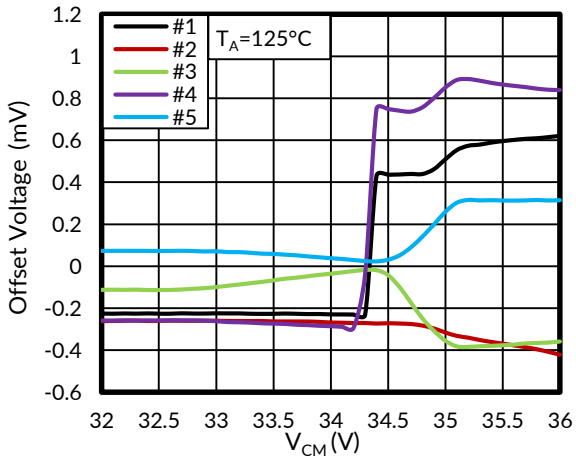


Figure 10. Offset Voltage vs Common Mode Voltage (Transition Region)

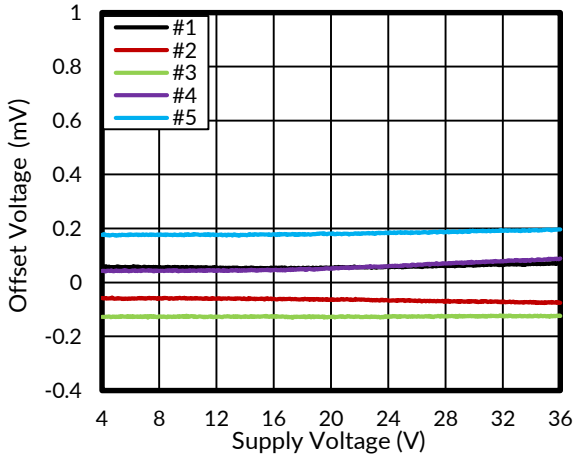


Figure 11. Offset Voltage vs Supply Voltage

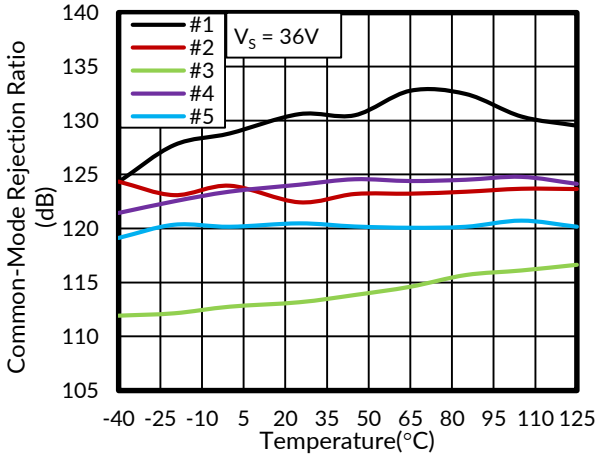


Figure 12. CMRR vs Temperature

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = +25°C, V_S = ±18V, V_{CM} = 0V, R_L = 10kΩ, unless otherwise specified.

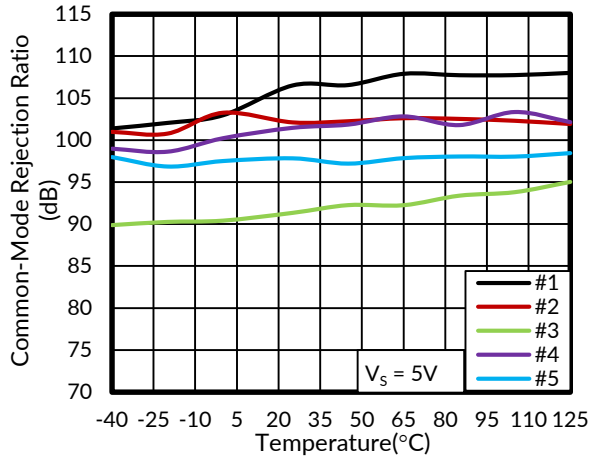


Figure 13. CMRR vs Temperature

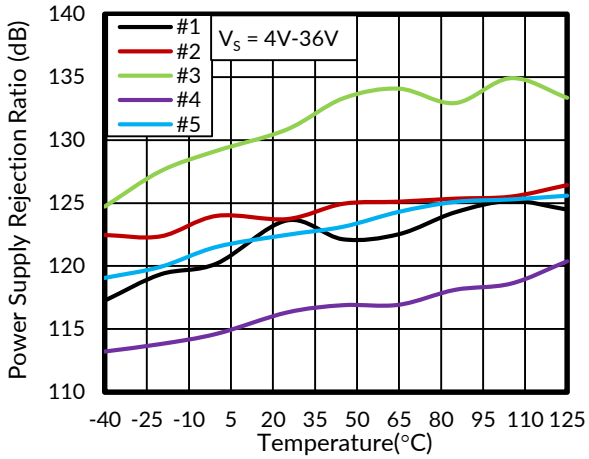


Figure 14. PSRR vs Temperature

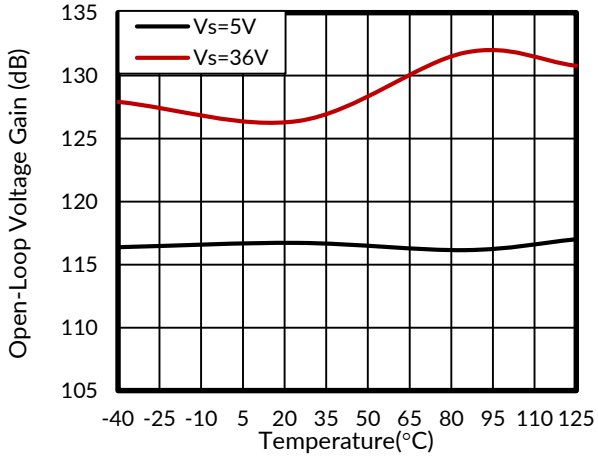


Figure 15. Open-Loop Voltage Gain vs Temperature

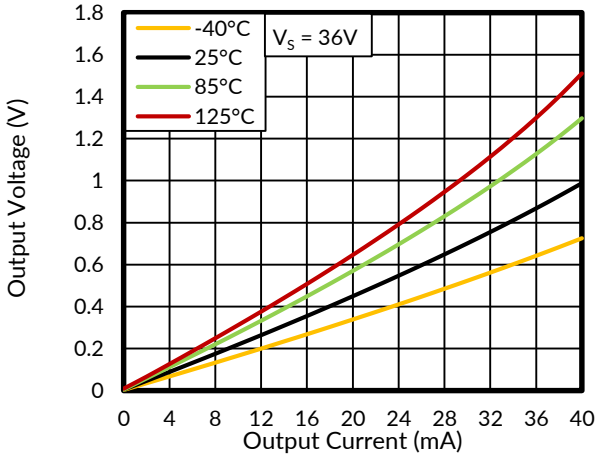


Figure 16. Output Swing from Positive Rail vs Output Current (Sourcing)

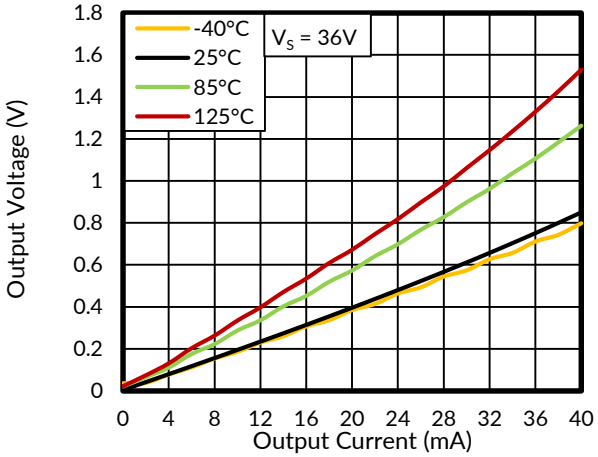


Figure 17. Output Swing from Negative Rail vs Output Current (Sinking)

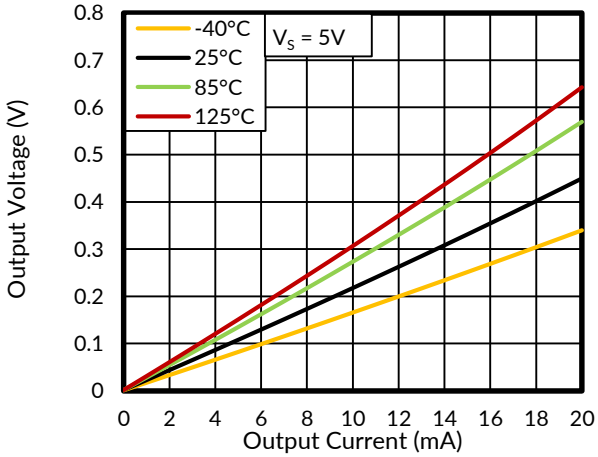


Figure 18. Output Swing from Positive Rail vs Output Current (Sourcing)

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = +25°C, V_S = ±18V, V_{CM} = 0V, R_L = 10kΩ, unless otherwise specified.

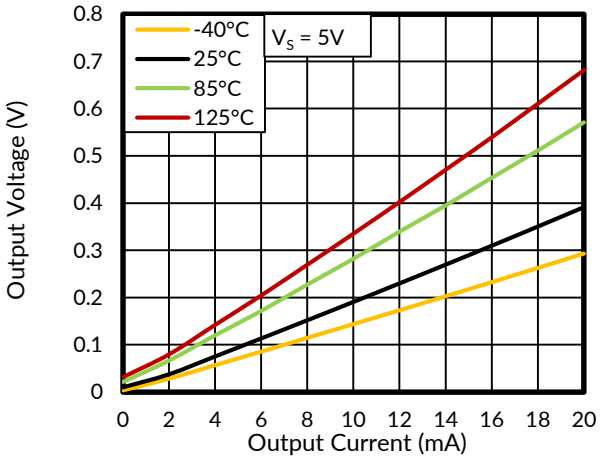


Figure 19. Output Swing from Negative Rail vs Output Current (Sinking)

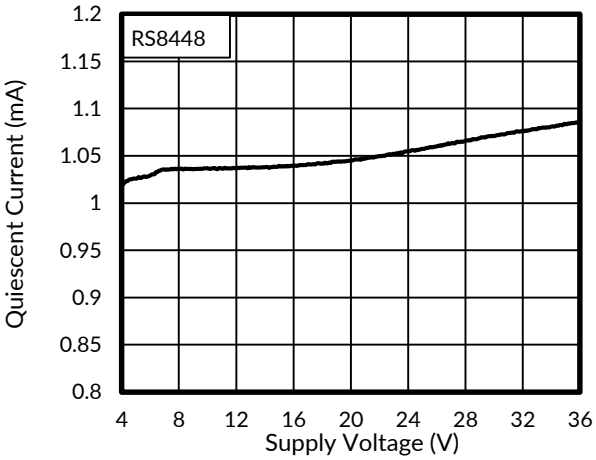


Figure 20. Quiescent Current vs Supply Voltage

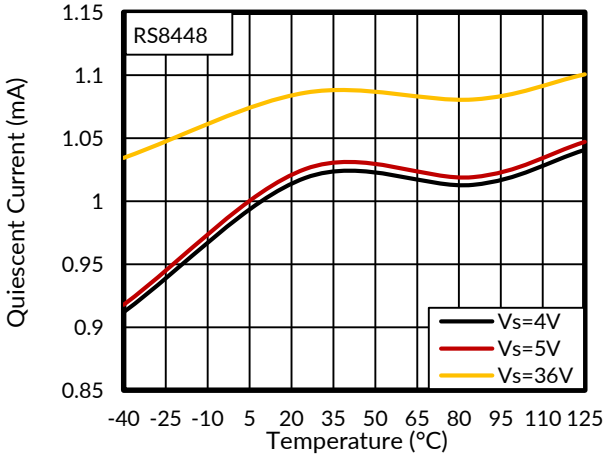


Figure 21. Quiescent Current vs Temperature

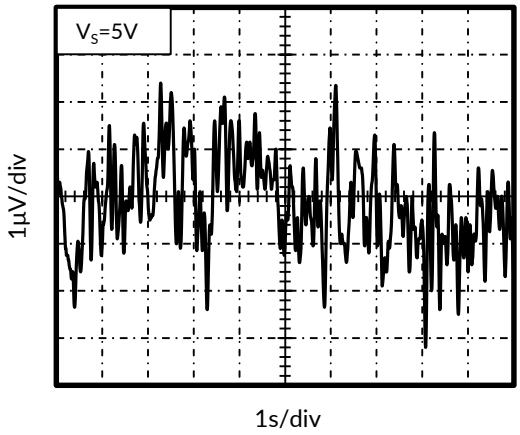


Figure 22. 0.1Hz to 10Hz Noise

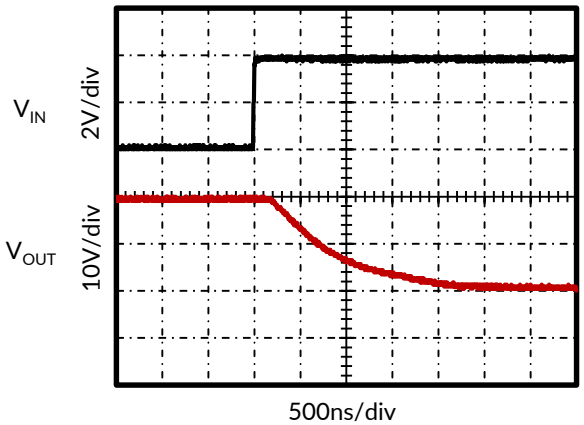


Figure 23. Positive Overload Recovery

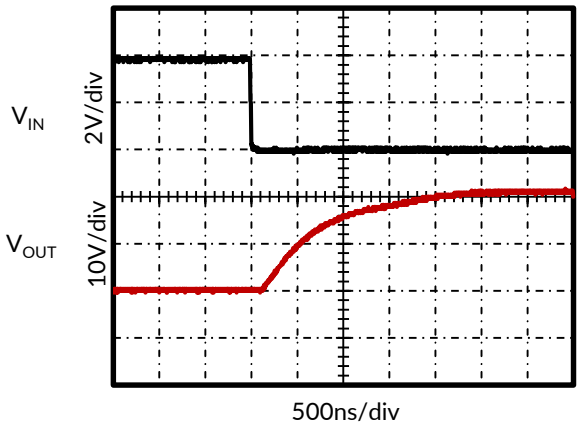


Figure 24. Negative Overload Recovery

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = +25°C, V_S = ±18V, V_{CM} = 0V, R_L = 10kΩ, unless otherwise specified.

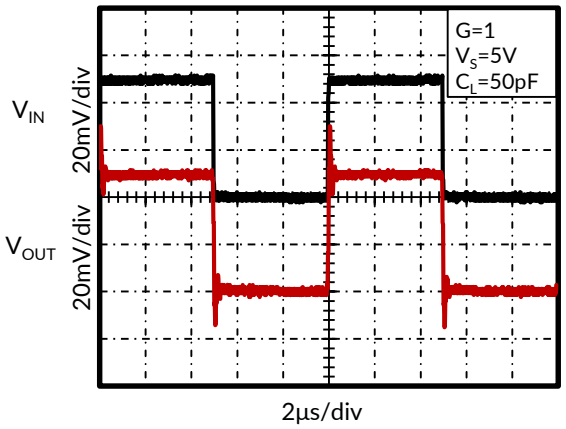


Figure 25. Small Signal Step Response

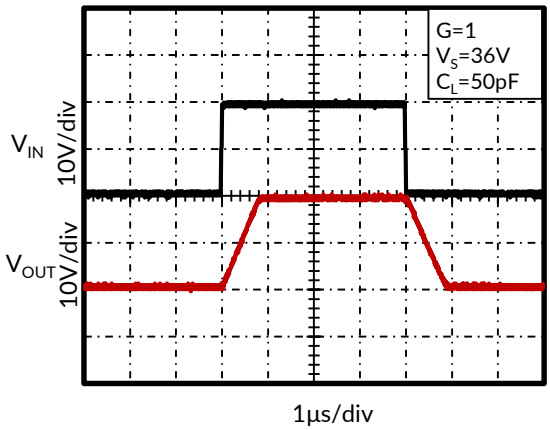


Figure 26. Large Signal Step Response

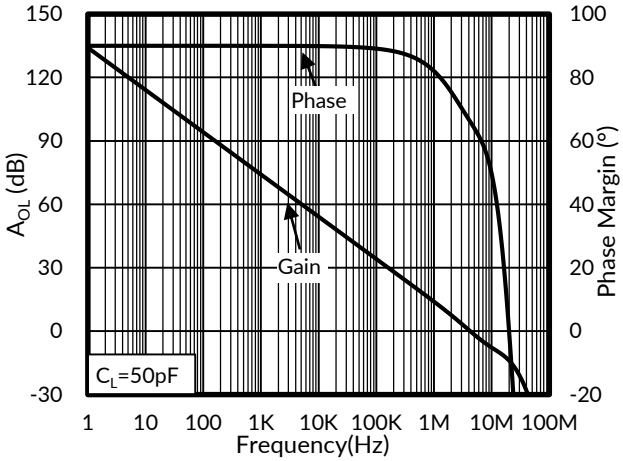


Figure 27. Open−Loop Gain and Phase vs Frequency

8 DETAILED DESCRIPTION

8.1 Input Protection Circuitry

The RS8447 and RS8448 uses a special input architecture to eliminate the requirement for input protection diodes but still provides robust input protection under transient conditions. Figure 28 shows conventional input diode protection schemes that are activated by fast transient step responses and introduce signal distortion and settling time delays because of alternate current paths, as shown in Figure 29. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, causing an increase in input current and resulting in extended settling time.

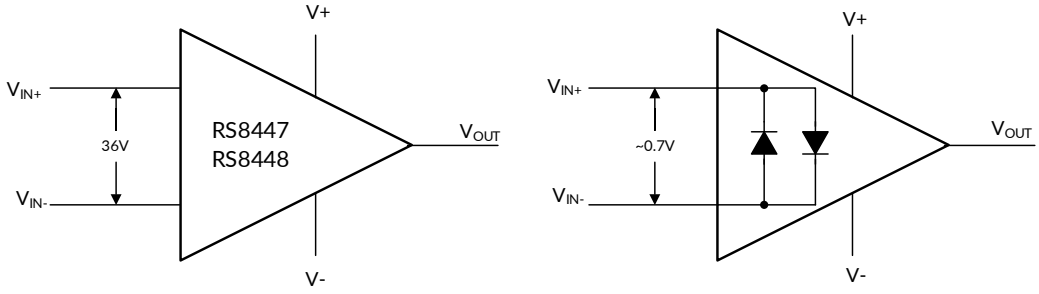


Figure 28. Input Protection Does Not Limit Differential Input Capability

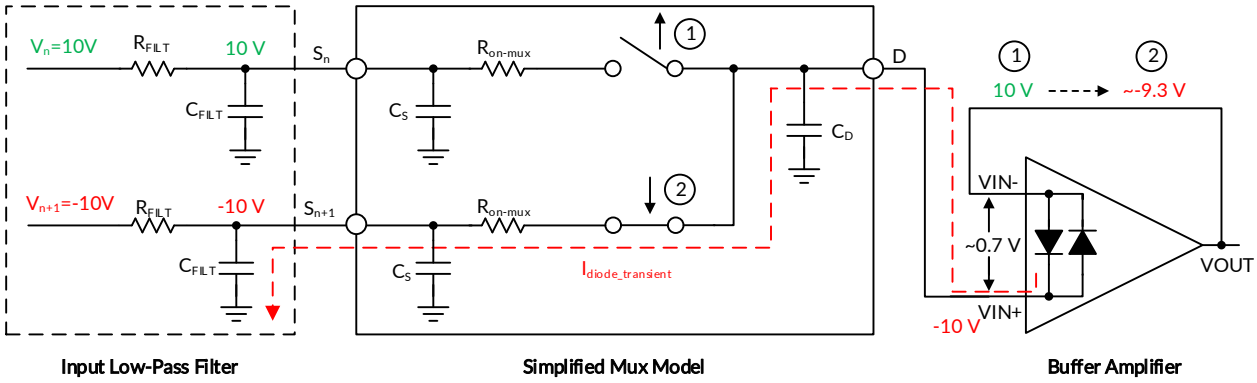


Figure 29. Back-to-Back Diodes Create Settling Issues

The RS8447 and RS8448 family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications using a patented input protection architecture that does not introduce additional signal distortion or delayed settling time, making the device an optimal op amp for multichannel, high-switched, input applications. The RS8447 and RS8448 tolerate a maximum differential swing (voltage between inverting and non-inverting pins of the op amp) of up to 36V, making the device suitable for use as a comparator or in applications with fast-ramping input signals such as data-acquisition systems.

8.2 Thermal Protection

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called self-heating. The absolute maximum junction temperature of the RS8447 and RS8448 is 150°C. Exceeding this temperature causes damage to the device. The RS8447 and RS8448 have a thermal protection feature that reduces damage from self-heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 160°C. Figure 30 shows an application example for the RS8447 that has significant self-heating. The actual device, however, turns off the output drive to recover towards a safe junction temperature. Figure 30 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3V. When self-heating causes the device junction temperature to increase above the internal limit, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor R_L. If the condition that

caused excessive power dissipation is not removed, the amplifier will oscillate between a shutdown and enabled state until the output fault is corrected.

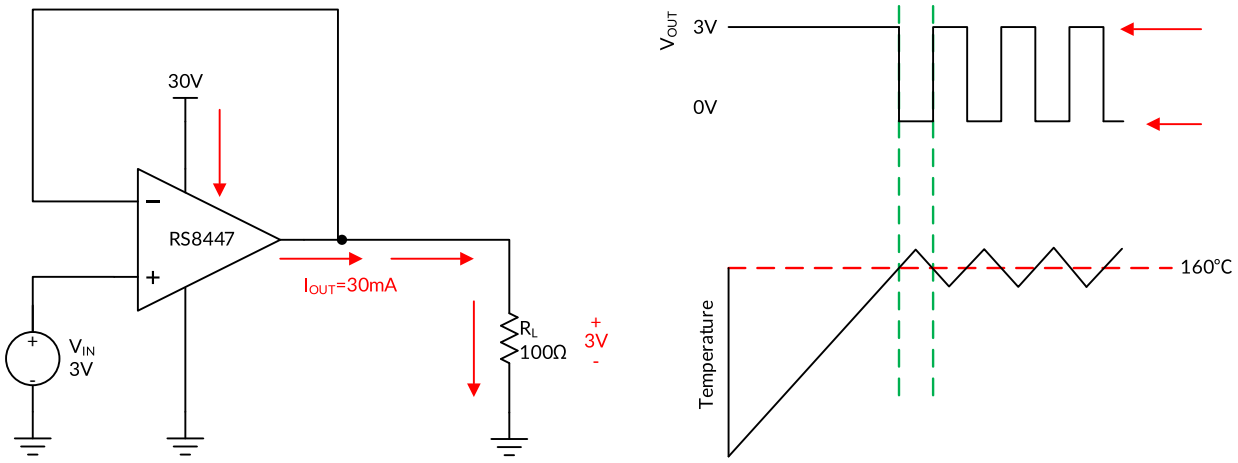


Figure 30. Thermal Protection

8.3 Common-Mode Voltage Range

The RS8447 and RS8448 are 36V, true rail-to-rail input operational amplifiers with an input common-mode range that extends to both supply rails. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in Figure 31. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1 V above the positive supply. The P-channel pair is active for inputs from the negative supply to approximately (V+) – 2.5V. There is a small transition region, typically (V+) – 2.5V to (V+) – 1V in which both input pairs are on. This transition region can vary modestly with process variation, and within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance may be degraded compared to operation outside this region.

Figure 5 shows this transition region for a typical device in terms of input voltage offset in more detail.

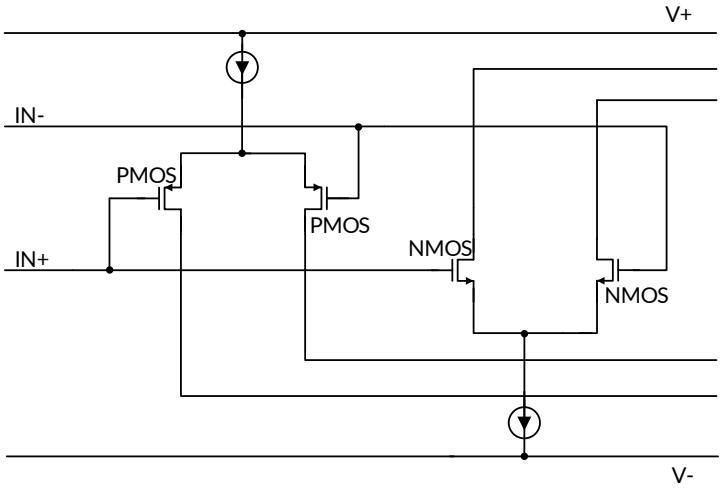


Figure 31. Rail-to-Rail Input Stage

8.4 Phase Reversal Protection

The RS8447 and RS8448 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in non-inverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The RS8447 and RS8448 are rail-to-rail input op amps; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in Figure 32.

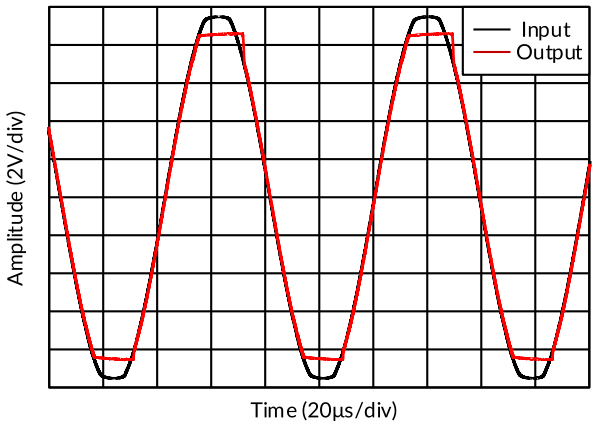


Figure 32. No Phase Reversal

9 APPLICATION AND IMPLEMENTATION

Information in the following applications sections is not part of the RUNIC component specification, and RUNIC does not warrant its accuracy or completeness. RUNIC's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Note

The RS8447 and RS8448 family offers excellent DC precision and AC performance. These devices operate up to 36V supply rails and offer true rail-to-rail input/output, low offset voltage and offset voltage drift, as well as 5MHz bandwidth and high output drive. These features make the RS8447 and RS8448 robust, high-performance operational amplifiers for high-voltage industrial applications.

9.2 Typical Applications

9.2.1 Slew Rate Limit for Input Protection

In control systems for valves or motors, abrupt changes in voltages or currents can cause mechanical damages. By controlling the slew rate of the command voltages into the drive circuits, the load voltages ramps up and down at a safe rate. For symmetrical slew-rate applications (positive slew rate equals negative slew rate), one additional op amp provides slew-rate control for a given analog gain stage. The unique input protection and high output current and slew rate of the RS8447 and RS8448 make the device an optimal amplifier to achieve slew rate control for both dual- and single-supply systems. Figure 33 shows the RS8447 and RS8448 in a slew-rate limit design.

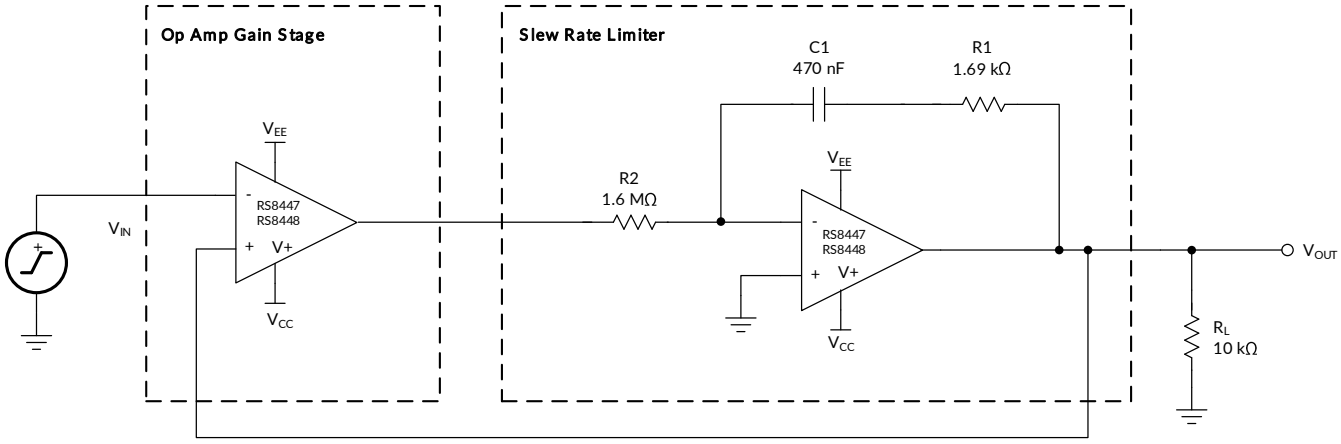


Figure 33. Slew Rate Limiter Uses One Op Amp

10 POWER SUPPLY RECOMMENDATIONS

The RS8447 and RS8448 are specified for operation from 4V to 36V (±2V to ±18V); many specifications apply from –40°C to 125°C or with specific supply voltages and test conditions. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the Typical Characteristics section.

Place 0.1μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the Layout section.

11 LAYOUT

11.1 Layout Guidelines

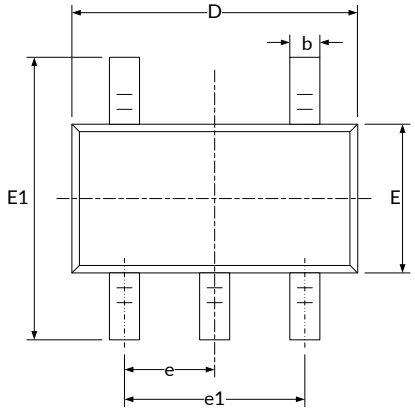
For best operational performance of the device, use good PCB layout practices, including:

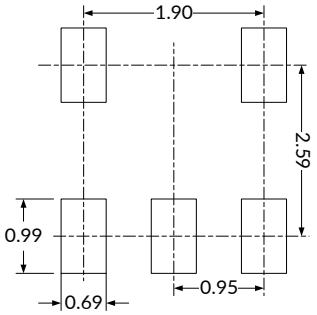
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.

Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

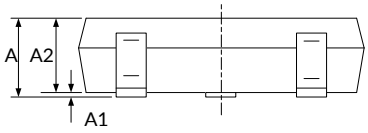
12 PACKAGE OUTLINE DIMENSIONS

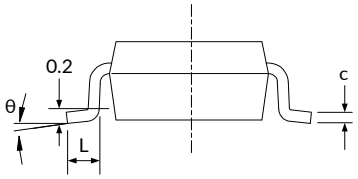
SOT23-5 (3)





RECOMMENDED LAND PATTERN (Unit: mm)



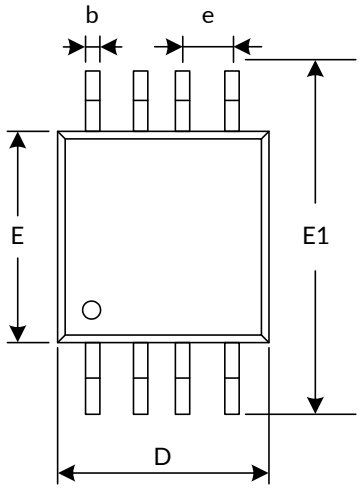


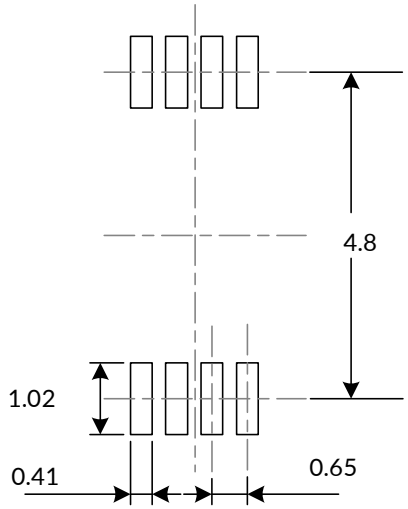
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D (1)	2.820	3.020	0.111	0.119
E (1)	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC) (2)		0.037(BSC) (2)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

NOTE:

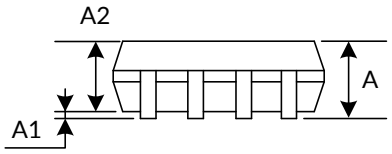
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

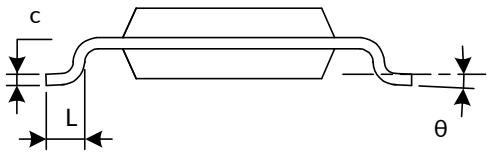
MSOP8 (3)





RECOMMENDED LAND PATTERN (Unit: mm)

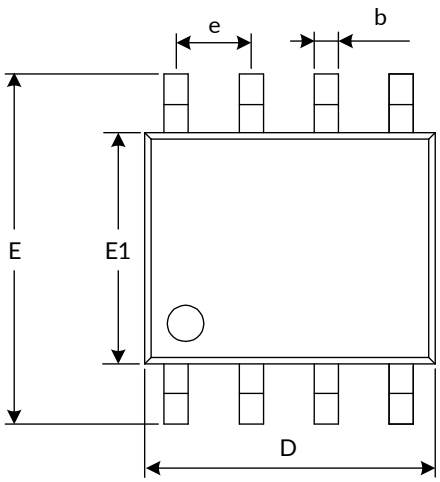


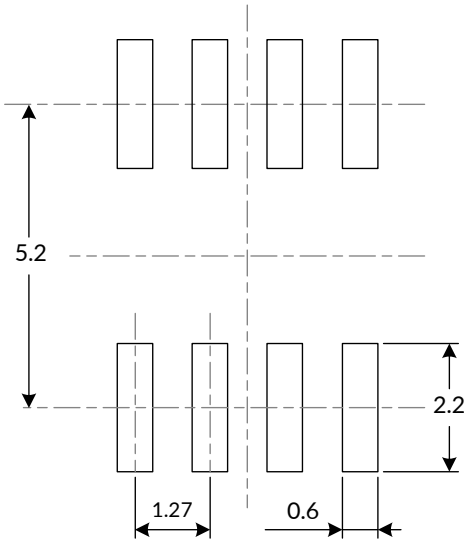


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D (1)	2.900	3.100	0.114	0.122
e	0.650(BSC) (2)		0.026(BSC) (2)	
E (1)	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

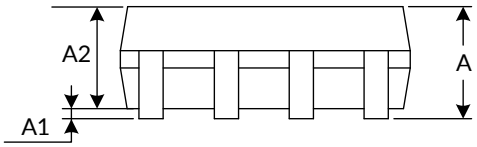
NOTE:
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

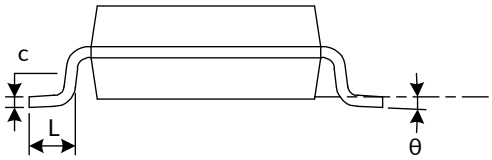
SOP8 (3)





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D (1)	4.800	5.000	0.189	0.197
e	1.270(BSC) (2)		0.050(BSC) (2)	
E	5.800	6.200	0.228	0.244
E1 (1)	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

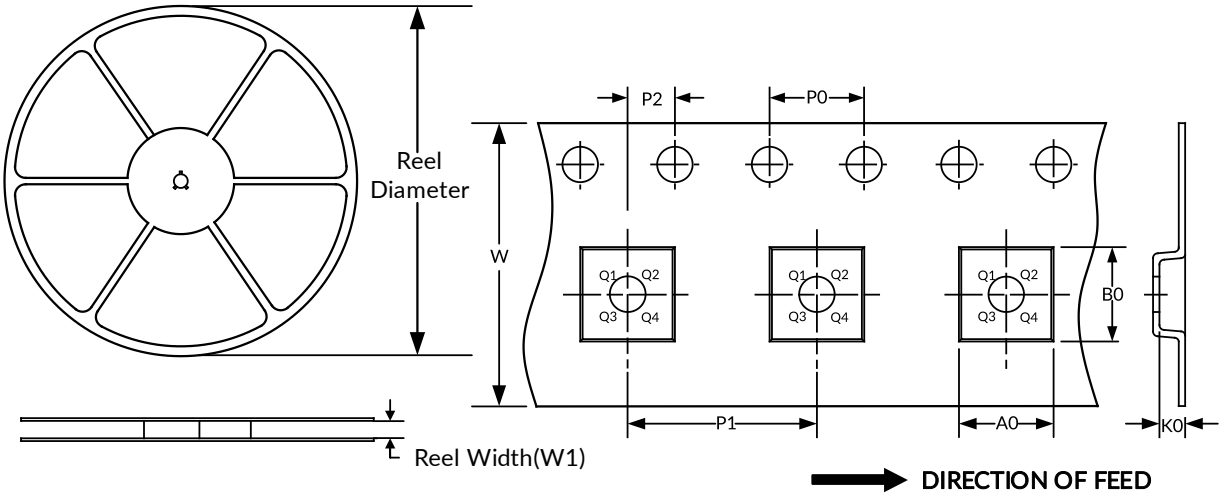
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

13 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT23-5	7”	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
MSOP8	13”	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1
SOP8	13”	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

IMPORTANT NOTICE AND DISCLAIMER

Jiangsu RUNIC Technology Co., Ltd. will accurately and reliably provide technical and reliability data (including data sheets), design resources (including reference designs), application or other design advice, WEB tools, safety information and other resources, without warranty of any defect, and will not make any express or implied warranty, including but not limited to the warranty of merchantability Implied warranty that it is suitable for a specific purpose or does not infringe the intellectual property rights of any third party.

These resources are intended for skilled developers designing with RUNIC products You will be solely responsible for: (1) Selecting the appropriate products for your application; (2) Designing, validating and testing your application; (3) Ensuring your application meets applicable standards and any other safety, security or other requirements; (4) RUNIC and the RUNIC logo are registered trademarks of RUNIC INCORPORATED. All trademarks are the property of their respective owners; (5) For change details, review the revision history included in any revised document. The resources are subject to change without notice. Our company will not be liable for the use of this product and the infringement of patents or third-party intellectual property rights due to its use.