5.5V, 6A, 18mΩ On-Resistance Dual-Channel Load Switch

1 FEATURES

- **Integrated Dual-Channel Load Switch**
- **Input voltage range: 0.6 V to V_{BIAS}**
- **V_{BIAS} Voltage Range: 2.5 V to 5.5 V**
- **On-Resistance**
  - **R_{ON} = 18 mΩ (Typical) at V_{IN} = 0.6 V to 5 V, V_{BIAS} = 5 V**
  - **R_{ON} = 23 mΩ (Typical) at V_{IN} = 0.6 V to 2.5 V, V_{BIAS} = 2.5 V**
- **6A Maximum Continuous Switch Current Per Channel**
- **Quiescent Current for RS2581**
  - **34µA (Typical, Both Channels) at V_{IN} = V_{BIAS} = 5V**
  - **30µA (Typical, Single Channel) at V_{IN} = V_{BIAS} = 5V**
- **Control Input Threshold Enables Use of 1.2V, 1.8V, 2.5V, and 3.3V logic**
- **Configurable Rise Time**
- **Thermal Shutdown**
- **DFN3X2-14 Package with Thermal Pad**
- **ESD Performance Tested per JESD 22**
  - **2kV HBM and 1kV CDM**

2 APPLICATIONS

- **PC and Notebooks**
- **Set-Top Boxes and Residential Gateways**
- **Telecom Systems**
- **Solid-State Drives (SSD)**

3 DESCRIPTIONS

The RS2581 device is a dual-channel load switch with controlled turn on, integrating N-channel MOSFET power devices to meet high-side load switch applications. The device can operate over an input voltage range of 0.6 V to 5.5 V, and can support a maximum continuous current of 6 A per channel. Each switch is independently controlled by an on and off input (ON1 and ON2), which can interface directly with low-voltage control signals. The RS2581 is capable of thermal shutdown when the junction temperature is above the threshold, turning the switch off. The switch turns on again when the junction temperature stabilizes to a safe range. The RS2581 also offers an optional integrated 220 Ω on-chip load resistor for quick output discharge when the switch is turned off.

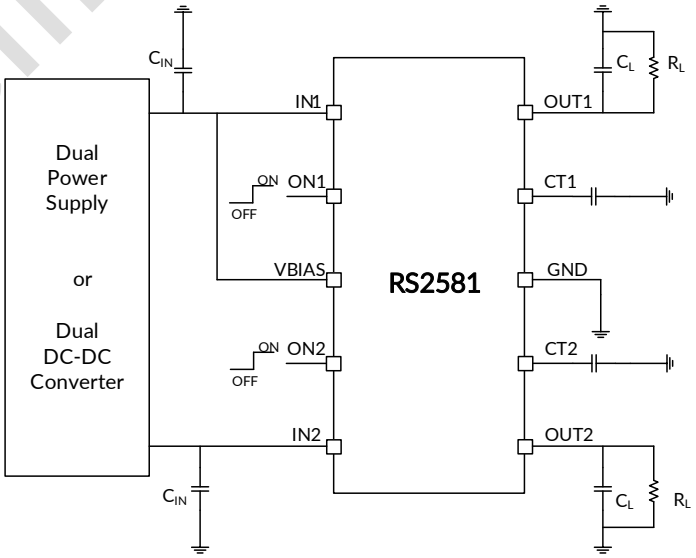
The RS2581 is available in a small, space-saving DFN3X2-14 package with integrated thermal pad allowing for high power dissipation. The device is characterized for operation over the free-air temperature range of -40°C to +105°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS2581	DFN3X2-14	3.00mm×2.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 TYPICAL APPLICATION CIRCUIT



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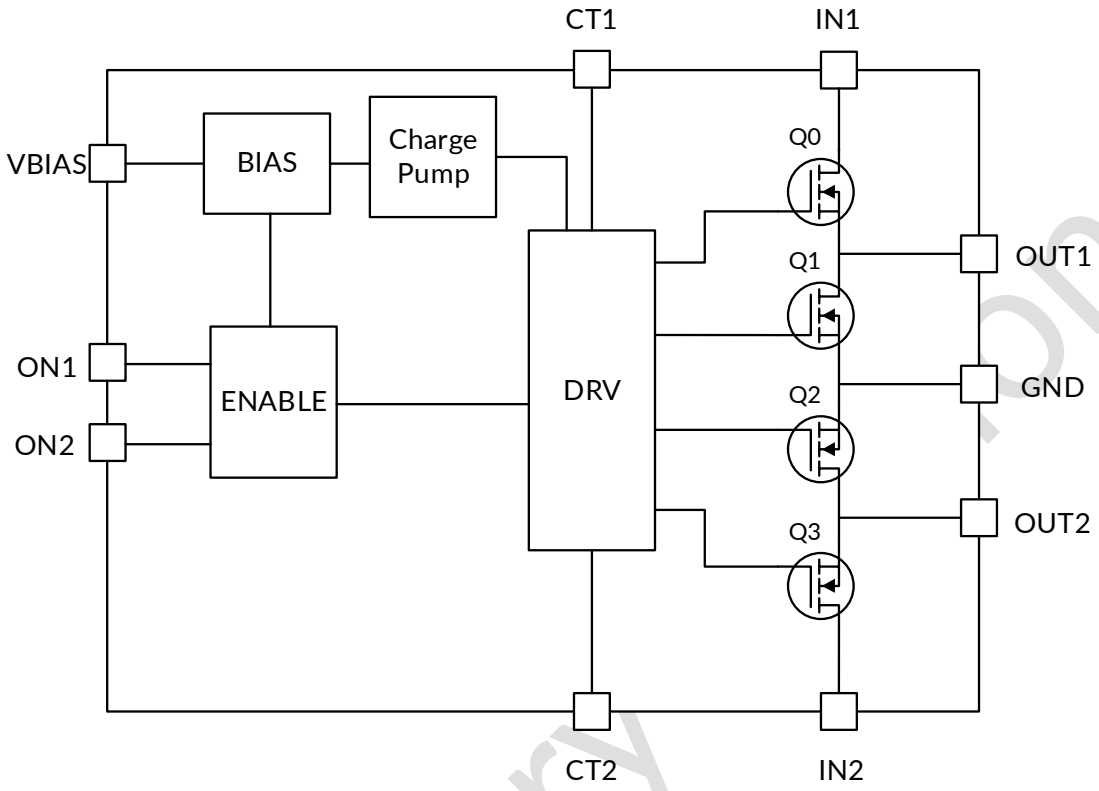
5 FUNCTIONAL BLOCK DIAGRAM



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6 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2025/06/17	Preliminary version completed
A.0.1	2025/07/23	Update Electrical Characteristics

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7 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2)	MSL (3)	PACKAGE OPTION
RS2581	RS2581XTDB14	-40°C ~+105°C	DFN3X2-14	2581	MSL3	Tape and Reel, 3000

NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

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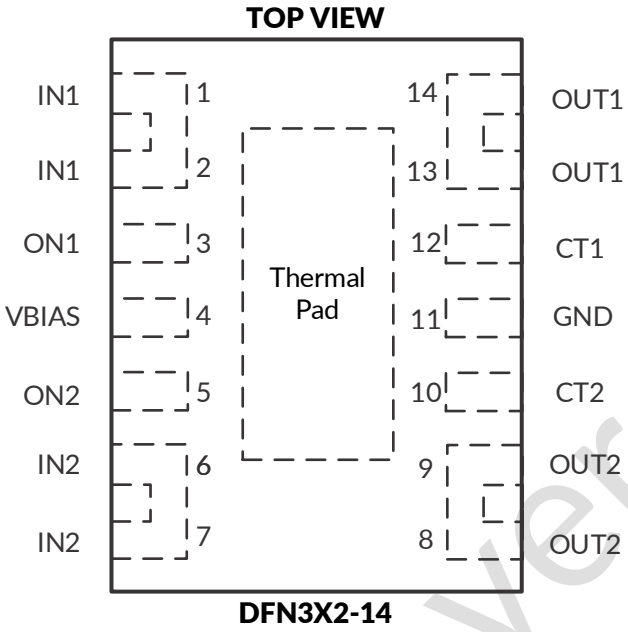
8 PIN CONFIGURATIONS



PIN		I/O (1)	DESCRIPTION
NAME	NO.		
IN1	1	I	Switch 1 input. Recommended voltage range for these pins for optimal Ron performance is 0.6V to V_{BIAS}. Place an optional decoupling capacitor between these pins and GND to reduce V_{IN1} dip during turn on of the channel.
	2		
ON1	3	I	Active-high switch 1 control input. Do not leave floating.
VBIAS	4	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5V to 5.5V.
ON2	5	I	Active-high switch 2 control input. Do not leave floating.
IN2	6	I	Switch 2 input. Recommended voltage range for these pins for optimal Ron performance is 0.6V to V_{BIAS}. Place an optional decoupling capacitor between these pins and GND to reduce V_{IN2} dip during turn on of the channel.
	7		
OUT2	8	O	Switch 2 output.
	9		
CT2	10	O	Switch 2 slew rate control. Can be left floating.
GND	11	-	Ground.
CT1	12	O	Switch 1 slew rate control. Can be left floating.
OUT1	13	O	Switch 1 output.
	14		
Thermal pad	-	-	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND.

(1) I=input, O=output.

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9 SPECIFICATIONS

9.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

			MIN	MAX	UNIT
$V_{IN1,2}$	Input Voltage		-0.3	5.8	V
$V_{OUT1,2}$	Output Voltage		-0.3	5.8	V
$V_{ON1,2}$	ON Pin Voltage		-0.3	5.8	V
V_{BIAS}	BIAS Voltage		-0.3	5.8	V
I_{MAX}	Maximum continuous current per channel			6	A
$I_{MAX,PLS}$	Maximum pulsed current switch per channel, pulse<300μs, 3% duty cycle			8	A
θ_{JA}	Package thermal impedance (3)	DFN3X2-14		60	°C/W
T_J	Operating junction temperature (4)			125	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the GND pin.
(3) The package thermal impedance is calculated in accordance with JESD-51.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

9.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), MIL-STD 883J	±2000	V
		Charge Device Model (CDM), ANSI/ESDA/JEDEC JS-002-2022	±1000	V

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{IN1,2}$	Input Voltage	0.6	V_{BIAS}	V
V_{BIAS}	BIAS Voltage	2.5	5.5	V
$V_{ON1,2}$	ON Pin Voltage	0	5.5	V
$V_{OUT1,2}$	Output Voltage	0	V_{IN}	V
V_{IH}	High-Level Input Voltage, ON	1.2	5.5	V
V_{IL}	Low-Level Input Voltage, ON	0	0.5	V
Operating Ambient Temperature, T_A		-40	105	°C

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9.4 Electrical Characteristics

(At V_{IN}=V_{BIAS}=5V, T_A=25°C, unless otherwise noted.)

PARAMETER		TEST CONDITIONS		TEMP	MIN(1)	TYP(2)	MAX(1)	UNIT
Power Supplies and Currents								
$I_{Q,VBIAS}$	V_{BIAS} Quiescent Current (both channels)	I_{OUT1}=I_{OUT2}=0mA, $V_{IN1,2}$=$V_{ON1,2}$=5V		-40°C to 105°C		34	45	μA
	V_{BIAS} Quiescent Current (single channels)	I_{OUT1}=I_{OUT2}=0mA, V_{ON2}=0, $V_{IN1,2}$=V_{ON1}=5V		-40°C to 105°C		30	40	μA
$I_{SD,VBIAS}$	V_{BIAS} Shutdown Current	$V_{ON1,2}$=0V, $V_{OUT1,2}$=0V		-40°C to 105°C		0.01	1	μA
$I_{SD,VIN}$	V_{IN} Shutdown Current (per channel)	V_{ON}=0V, V_{OUT}=0V	V_{IN}=5V	-40°C to 105°C		0.01	5	μA
			V_{IN}=3.3V	-40°C to 105°C		0.01	5	μA
			V_{IN}=1.8V	-40°C to 105°C		0.01	5	μA
			V_{IN}=0.6V	-40°C to 105°C		0.01	4.5	μA
I_{ON}	ON Pin Leakage Current	V_{ON}=5.5V		-40°C to 105°C		0.01	0.1	μA
Resistance Characteristics								
R_{ON}	On-Resistance	I_{OUT}=-200mA	V_{IN}=5V	25°C		18	21	mΩ
				-40°C to 85°C			24	mΩ
				-40°C to 105°C			25	mΩ
			V_{IN}=3.3V	25°C		17	20	mΩ
				-40°C to 85°C			23	mΩ
				-40°C to 105°C			25	mΩ
			V_{IN}=1.8V	25°C		19	22	mΩ
				-40°C to 85°C			23	mΩ
				-40°C to 105°C			24	mΩ
			V_{IN}=1.2V	25°C		18	21	mΩ
				-40°C to 85°C			24	mΩ
				-40°C to 105°C			25	mΩ
			V_{IN}=1.05V	25°C		18	21	mΩ
				-40°C to 85°C			23	mΩ
				-40°C to 105°C			25	mΩ
			V_{IN}=0.6V	25°C		17	20	mΩ
				-40°C to 85°C			23	mΩ
				-40°C to 105°C			25	mΩ
Enable Threshold Characteristics								
$V_{ON,THH}$	Input Logic-High Voltage, ON			-40°C to 105°C	1.2		5.5	V
$V_{ON,THL}$	Input Logic-Low Voltage, ON			-40°C to 105°C			0.5	V
$V_{ON,HYS}$	ON Pin Hysteresis			25°C		100		mV
OUT Characteristics								
R_{PD}	Output Pulldown Resistance	V_{IN}=5V		-40°C to 105°C		220	250	Ω
Thermal Protection								
T_{TSD}	Thermal Shutdown Junction Temperature Threshold					170		°C
T_{TSD_HYS}	Thermal Shutdown Junction Temperature Hysteresis					25		°C

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

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Electrical Characteristics

(At V_{IN}=V_{BIAS}=2.5V, T_A=25°C, unless otherwise noted.)

PARAMETER		TEST CONDITIONS		TEMP	MIN(1)	TYP(2)	MAX(1)	UNIT
Power Supplies and Currents								
$I_{Q,VBIAS}$	V_{BIAS} Quiescent Current (both channels)	I_{OUT1}=I_{OUT2}=0mA, $V_{IN1,2}$=$V_{ON1,2}$=2.5V		-40°C to 105°C		45	60	μA
	V_{BIAS} Quiescent Current (single channels)	I_{OUT1}=I_{OUT2}=0mA, V_{ON2}=0, $V_{IN1,2}$=V_{ON1}=2.5V		-40°C to 105°C		42	55	μA
$I_{SD,VBIAS}$	V_{BIAS} Shutdown Current	$V_{ON1,2}$=0V, $V_{OUT1,2}$=0V		-40°C to 105°C		0.01	1	μA
$I_{SD,VIN}$	V_{IN} Shutdown Current (per channel)	V_{ON}=0V, V_{OUT}=0V	V_{IN}=2.5V	-40°C to 105°C		0.01	5	μA
			V_{IN}=1.8V	-40°C to 105°C		0.01	5	μA
			V_{IN}=1.05V	-40°C to 105°C		0.01	5	μA
			V_{IN}=0.6V	-40°C to 105°C		0.01	4.5	μA
I_{ON}	ON Pin Leakage Current	V_{ON}=5.5V		-40°C to 105°C		0.01	0.1	μA
Resistance Characteristics								
R_{ON}	On-Resistance	I_{OUT}=-200mA	V_{IN}=2.5V	25°C		23	26	mΩ
				-40°C to 85°C			30	mΩ
				-40°C to 105°C			32	mΩ
			V_{IN}=1.8V	25°C		20	23	mΩ
				-40°C to 85°C			28	mΩ
				-40°C to 105°C			29	mΩ
			V_{IN}=1.5V	25°C		20	23	mΩ
				-40°C to 85°C			26	mΩ
				-40°C to 105°C			28	mΩ
			V_{IN}=1.2V	25°C		19	22	mΩ
				-40°C to 85°C			25	mΩ
				-40°C to 105°C			27	mΩ
			V_{IN}=1.05V	25°C		19	22	mΩ
				-40°C to 85°C			25	mΩ
				-40°C to 105°C			27	mΩ
			V_{IN}=0.6V	25°C		18	21	mΩ
				-40°C to 85°C			25	mΩ
				-40°C to 105°C			26	mΩ
Enable Threshold Characteristics								
$V_{ON,THH}$	Input Logic-High Voltage, ON			-40°C to 105°C	1.2		5.5	V
$V_{ON,THL}$	Input Logic-Low Voltage, ON			-40°C to 105°C			0.5	V
$V_{ON,HYS}$	ON Pin Hysteresis			25°C		50		mV
OUT Characteristics								
R_{PD}	Output Pulldown Resistance	V_{IN}=2.5V		-40°C to 105°C		230	250	Ω
Thermal Protection								
T_{TSD}	Thermal Shutdown Junction Temperature Threshold					170		°C
T_{TSD_HYS}	Thermal Shutdown Junction Temperature Hysteresis					25		°C

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

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9.5 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BIAS} = V_{ON} = V_{IN} = 5V, T_A=25°C (unless otherwise noted)						
t_{ON}	Turn On Time	R_L = 10 Ω, C_L = 0.1μF, C_T = 1000 pF		1160		μs
t_{OFF}	Turn Off Time	R_L = 10 Ω, C_L = 0.1μF, C_T = 1000 pF		2		
t_R	Rise Time	R_L = 10 Ω, C_L = 0.1μF, C_T = 1000 pF		1890		
t_F	Fall Time	R_L = 10 Ω, C_L = 0.1μF, C_T = 1000 pF		2		
t_D	Delay Time	R_L = 10 Ω, C_L = 0.1μF, C_T = 1000 pF		225		
V_{BIAS} = V_{ON} = 5V, V_{IN} = 0.6V, T_A=25°C (unless otherwise noted)						
t_{ON}	Turn On Time	R_L = 10 Ω, C_L = 0.1μF, C_T = 1000 pF		150		μs
t_{OFF}	Turn Off Time	R_L = 10 Ω, C_L = 0.1μF, C_T = 1000 pF		2.5		
t_R	Rise Time	R_L = 10 Ω, C_L = 0.1μF, C_T = 1000 pF		175		
t_F	Fall Time	R_L = 10 Ω, C_L = 0.1μF, C_T = 1000 pF		1.5		
t_D	Delay Time	R_L = 10 Ω, C_L = 0.1μF, C_T = 1000 pF		80		
V_{BIAS} = 2.5V, V_{ON} = 5V, V_{IN} = 2.5V, T_A=25°C (unless otherwise noted)						
t_{ON}	Turn On Time	R_L = 10 Ω, C_L = 0.1μF, C_T = 1000 pF		615		μs
t_{OFF}	Turn Off Time	R_L = 10 Ω, C_L = 0.1μF, C_T = 1000 pF		3		
t_R	Rise Time	R_L = 10 Ω, C_L = 0.1μF, C_T = 1000 pF		980		
t_F	Fall Time	R_L = 10 Ω, C_L = 0.1μF, C_T = 1000 pF		2		
t_D	Delay Time	R_L = 10 Ω, C_L = 0.1μF, C_T = 1000 pF		135		
V_{BIAS} = 2.5V, V_{ON} = 5V, V_{IN} = 0.6V, T_A=25°C (unless otherwise noted)						
t_{ON}	Turn On Time	R_L = 10 Ω, C_L = 0.1μF, C_T = 1000 pF		160		μs
t_{OFF}	Turn Off Time	R_L = 10 Ω, C_L = 0.1μF, C_T = 1000 pF		3.5		
t_R	Rise Time	R_L = 10 Ω, C_L = 0.1μF, C_T = 1000 pF		185		
t_F	Fall Time	R_L = 10 Ω, C_L = 0.1μF, C_T = 1000 pF		1.5		
t_D	Delay Time	R_L = 10 Ω, C_L = 0.1μF, C_T = 1000 pF		95		

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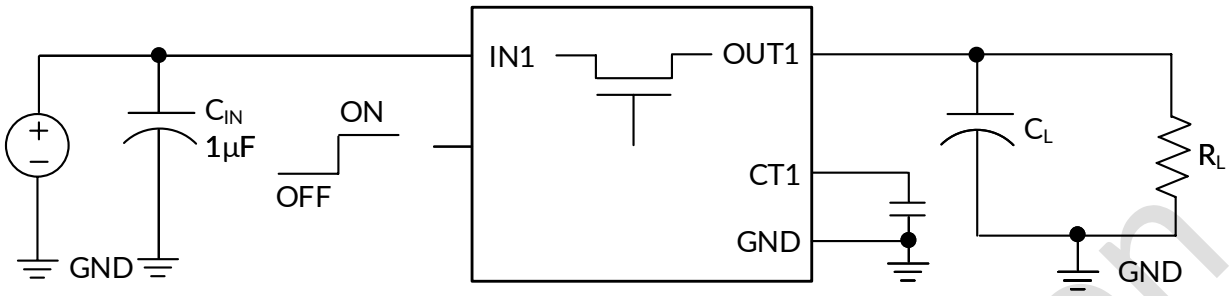
9.6 Parameter Measurement Information



(Single channel shown for clarity)

Figure 1. Test circuit

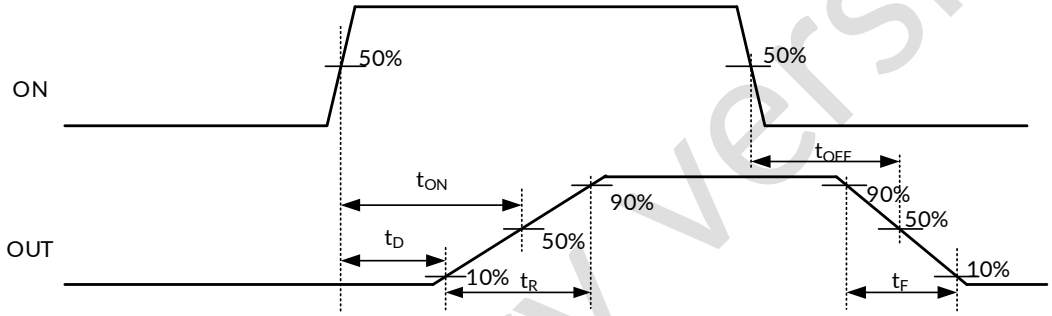


Figure 2. t_{ON} and t_{OFF} Waveforms

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9.7 Typical Performance Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

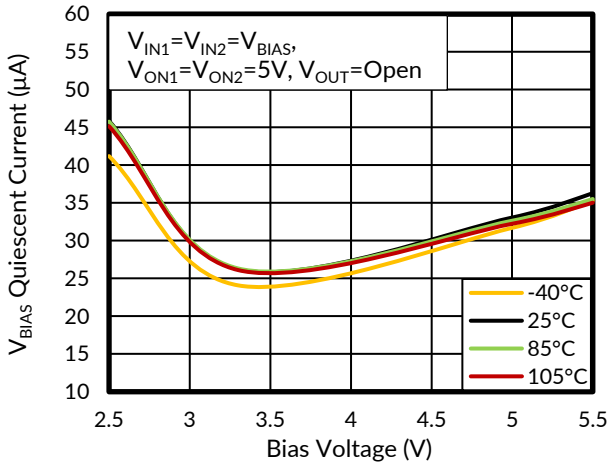

Figure 3. V_{BIAS} Quiescent Current vs Bias Voltage Both Channels

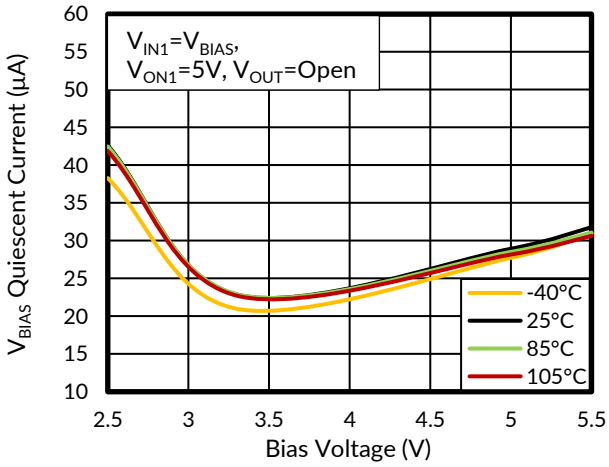

Figure 4. V_{BIAS} Quiescent Current vs Bias Voltage Single Channel

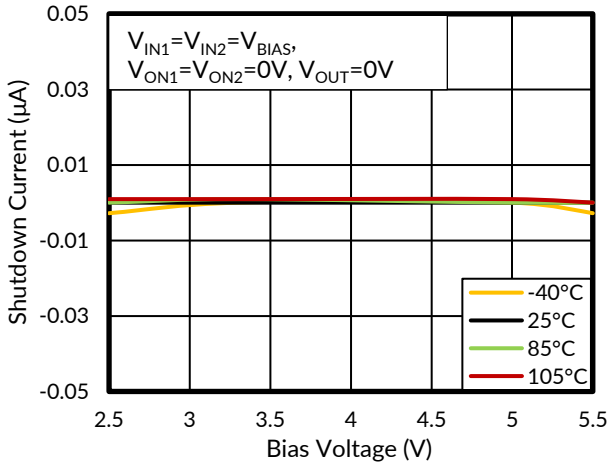

Figure 5. V_{BIAS} Shutdown Current vs Bias Voltage Both Channels

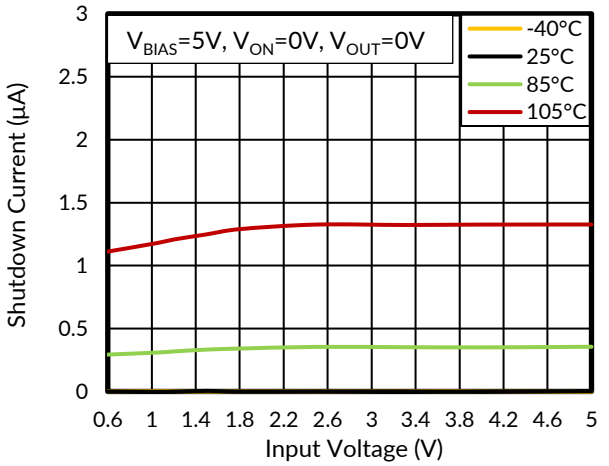

Figure 6. Off-State V_{IN} Current vs Input Voltage Single Channel

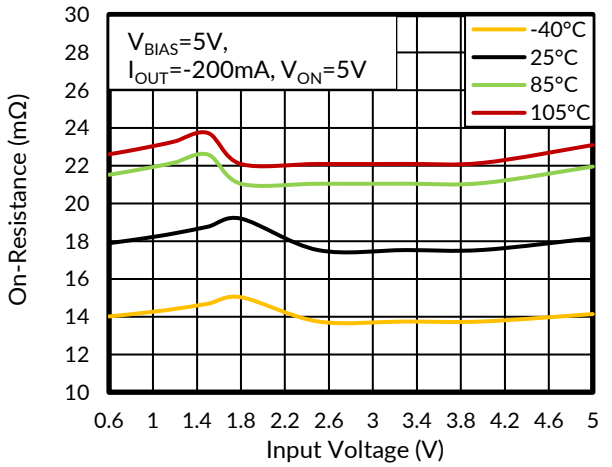

Figure 7. On-Resistance vs Input Voltage Single Channel - Across Ambient Temperatures

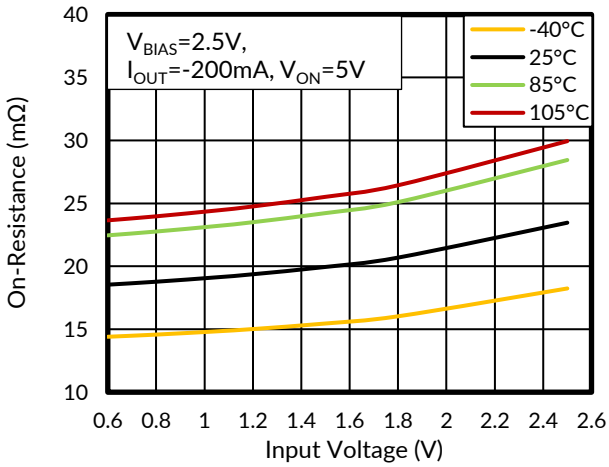

Figure 8. On-Resistance vs Input Voltage Single Channel - Across Ambient Temperatures

Typical Performance Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

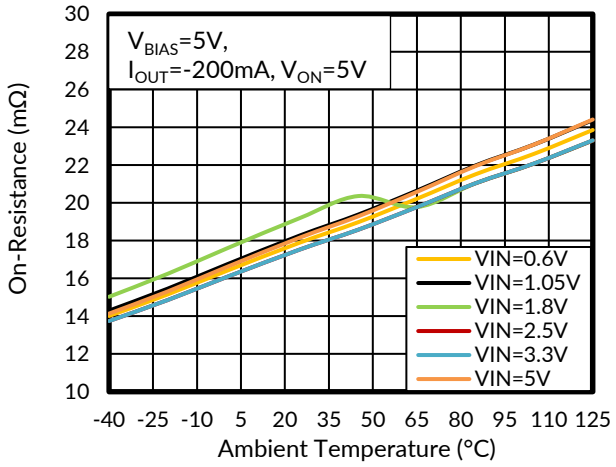

Figure 9. On-Resistance vs Ambient Temperature Single Channel

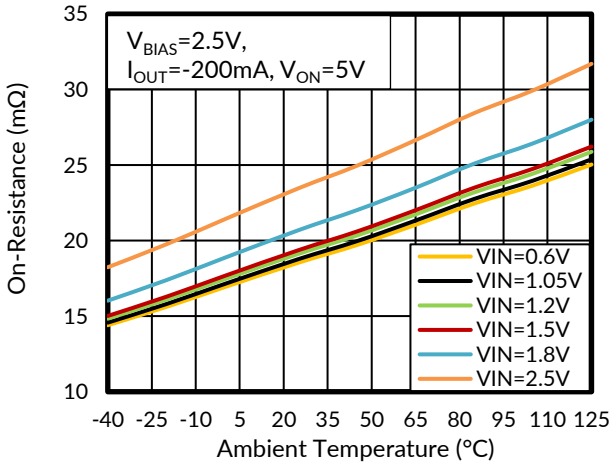

Figure 10. On-Resistance vs Ambient Temperature Single Channel

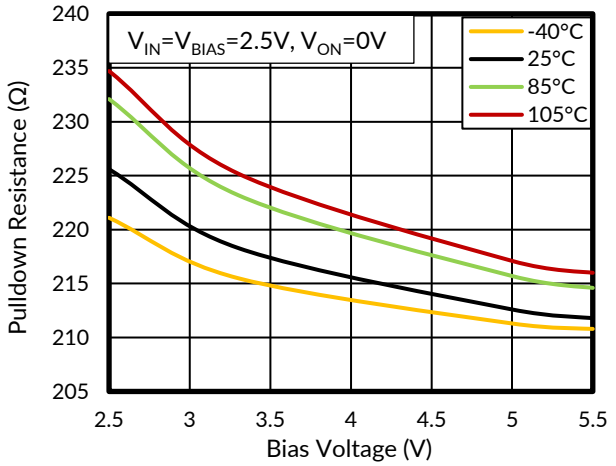

Figure 11. Pulldown Resistance vs Bias Voltage Single Channel

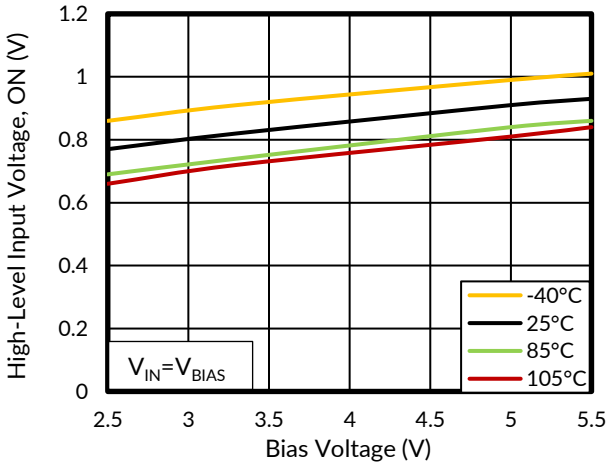

Figure 12. High-Level Input Voltage vs Bias Voltage

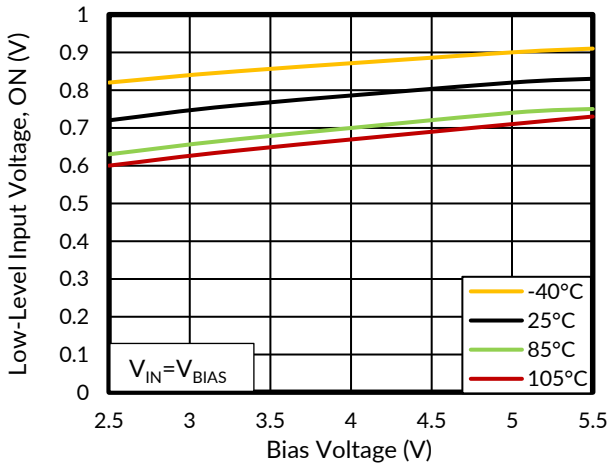

Figure 13. Low-Level Input Voltage vs Bias Voltage

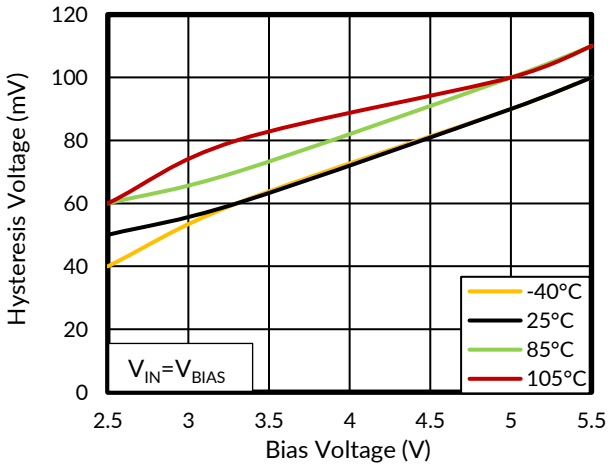

Figure 14. Voltage Input Hysteresis vs Bias Voltage

Typical Performance Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

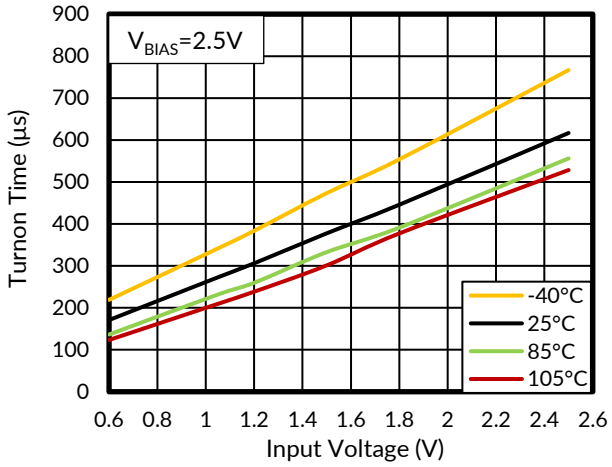

Figure 15. t_{ON} vs Input Voltage

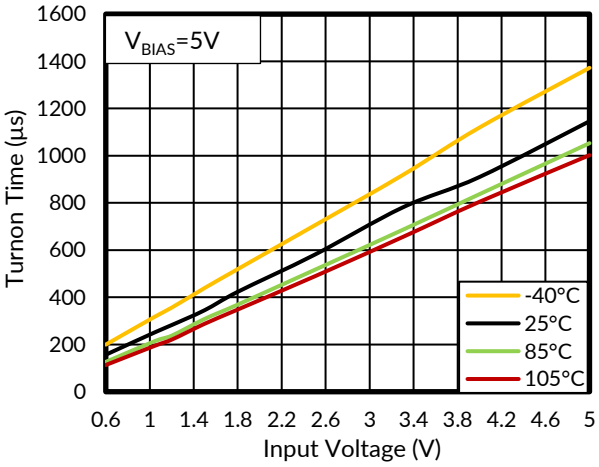

Figure 16. t_{ON} vs Input Voltage

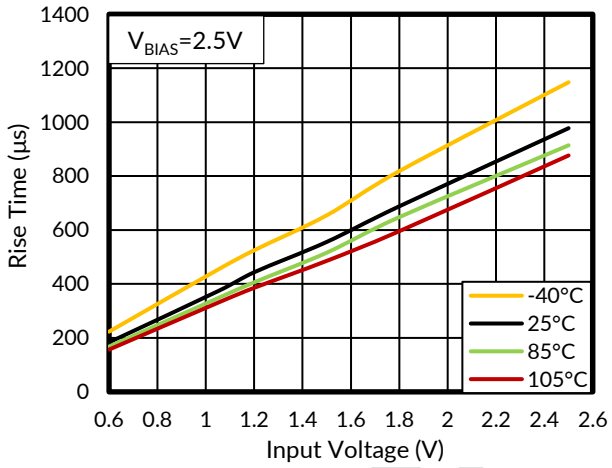

Figure 17. t_R vs Input Voltage

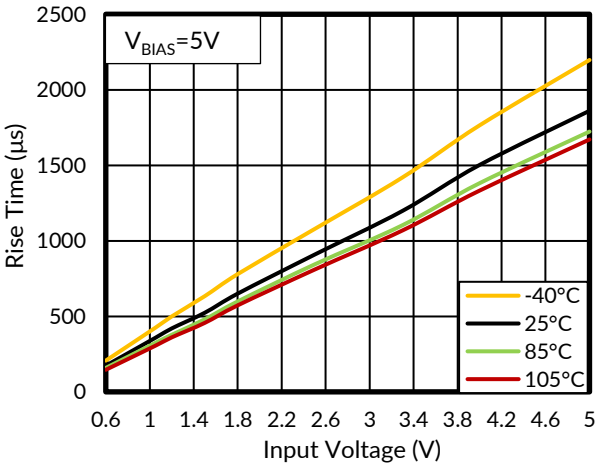

Figure 18. t_R vs Input Voltage

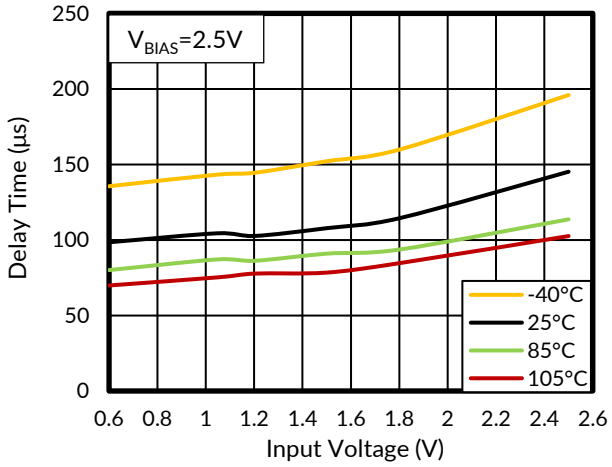

Figure 19. t_D vs Input Voltage

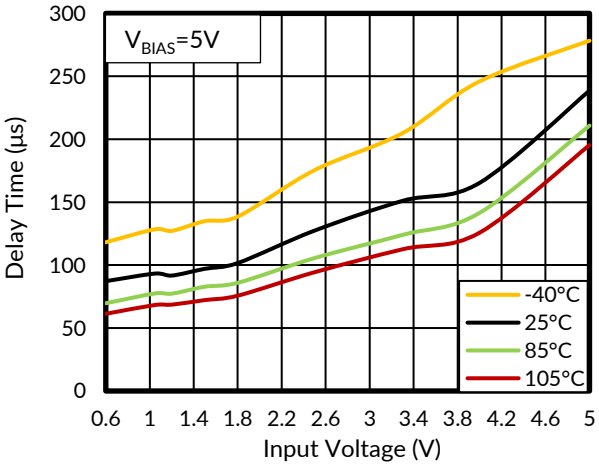

Figure 20. t_D vs Input Voltage

Typical Performance Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

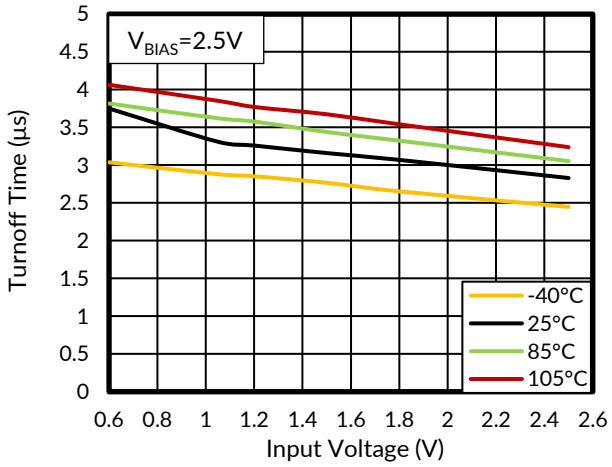

Figure 21. t_{OFF} vs Input Voltage

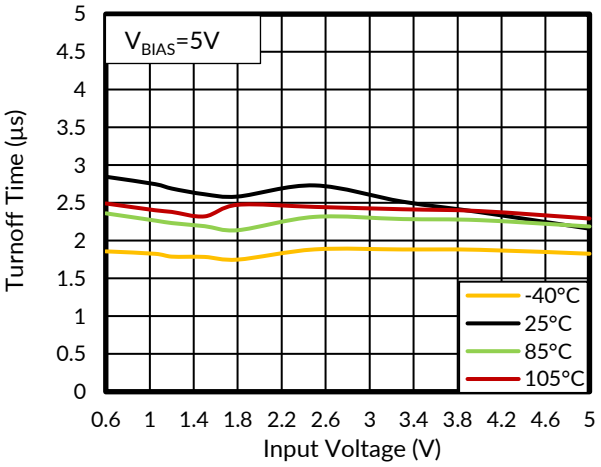

Figure 22. t_{OFF} vs Input Voltage

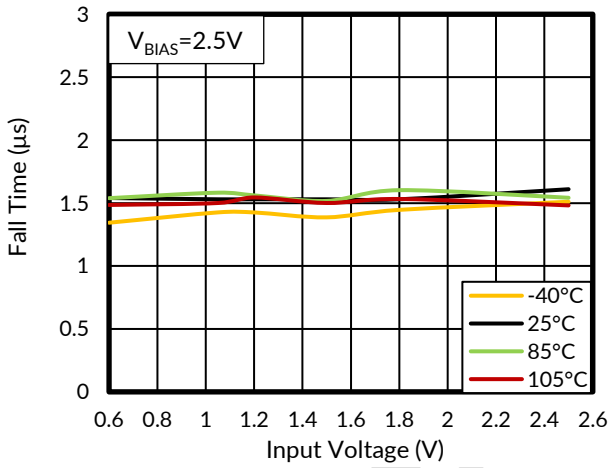

Figure 23. t_F vs Input Voltage

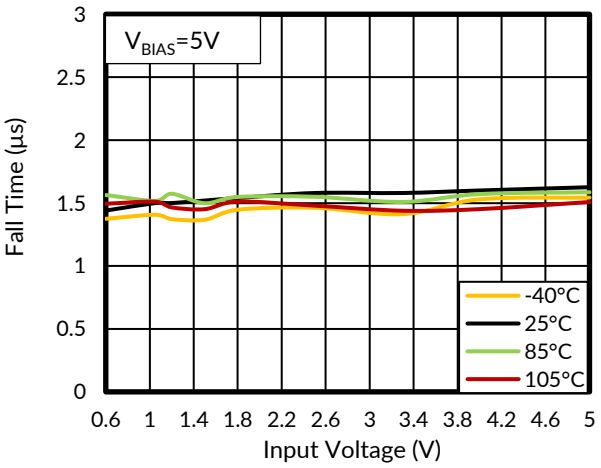

Figure 24. t_F vs Input Voltage

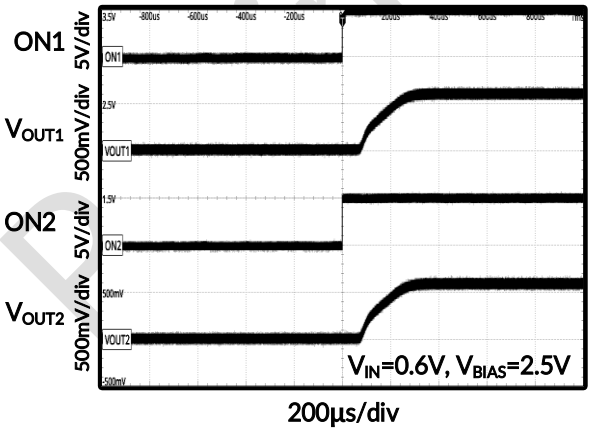

Figure 25. Turnon Response Time

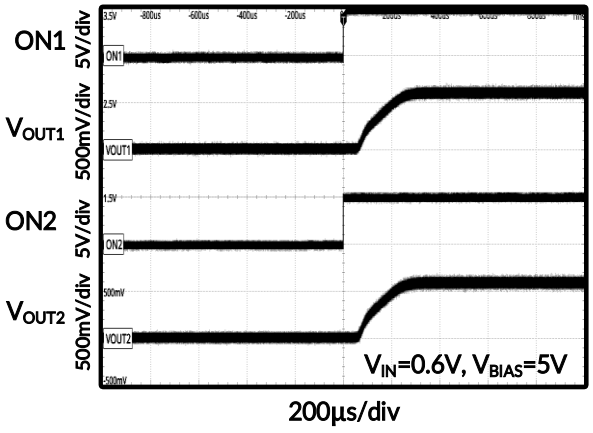

Figure 26. Turnon Response Time

Typical Performance Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

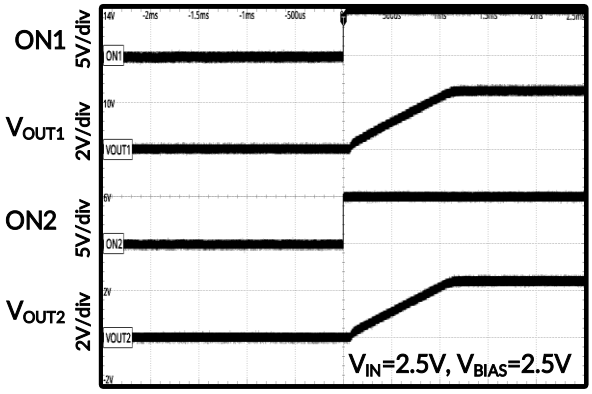

Figure 27. Turnon Response Time

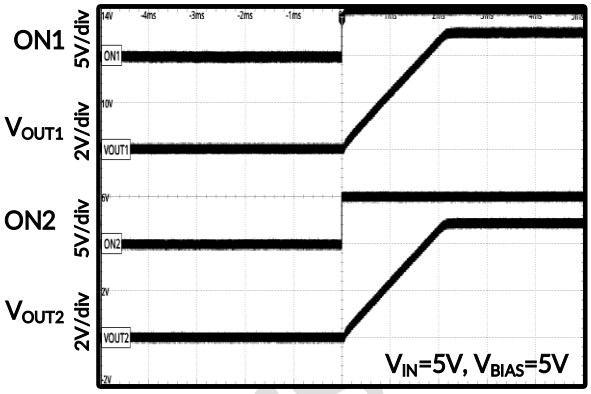

Figure 28. Turnon Response Time

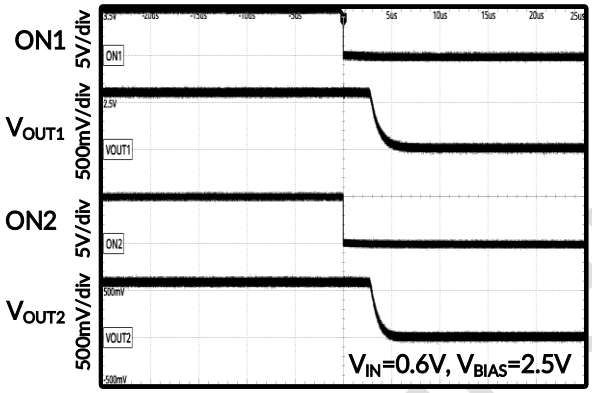

Figure 29. Turnoff Response Time

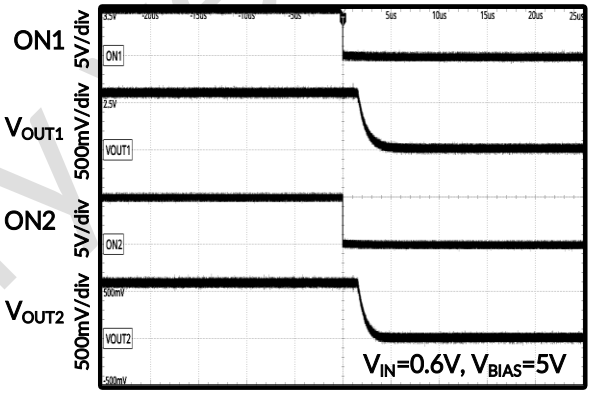

Figure 30. Turnoff Response Time

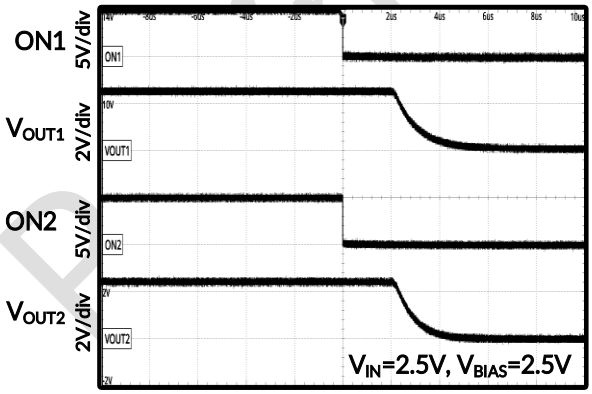

Figure 31. Turnoff Response Time

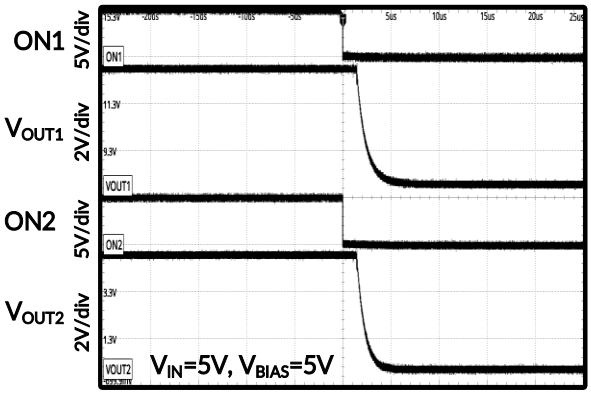

Figure 32. Turnoff Response Time

Preliminary

Typical Performance Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

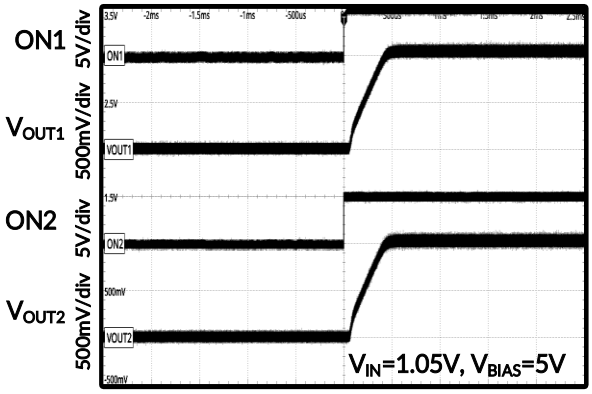

Figure 33. Turnon Response Time

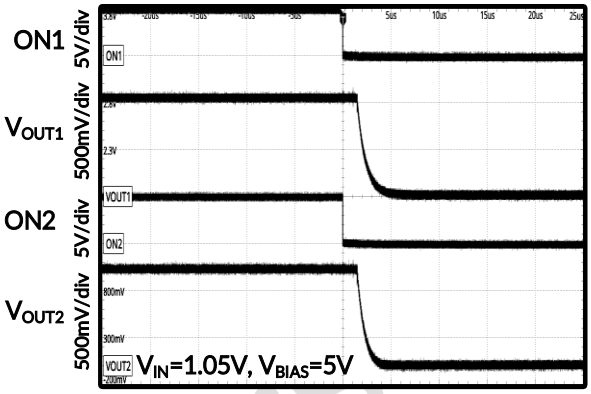

Figure 34. Turnoff Response Time

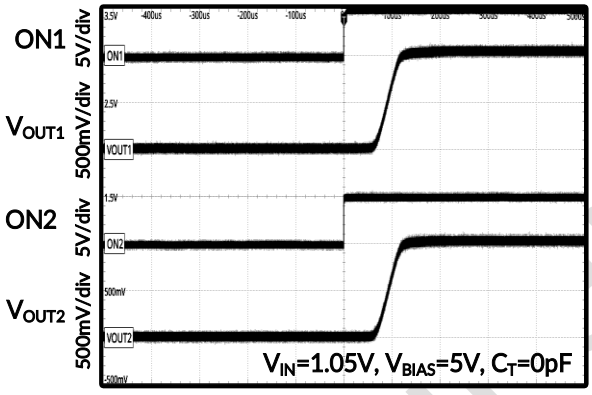

Figure 35. Turnon Response Time

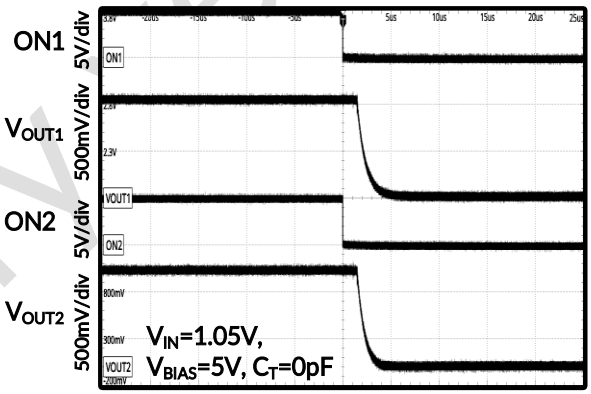

Figure 36. Turnoff Response Time

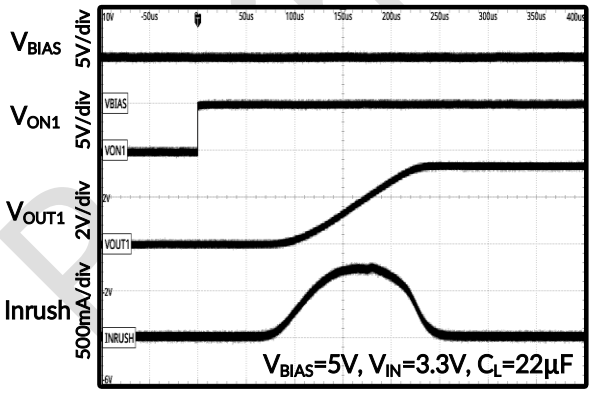

Figure 37. Inrush Current With C_T = 0 pF

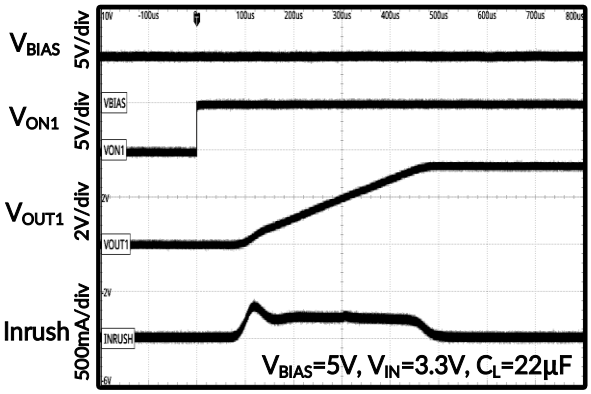

Figure 38. Inrush Current With C_T = 220 pF

Preliminary

10 FUNCTIONAL DESCRIPTION

10.1 Overview

The RS2581 device is a dual-channel load switch with controlled turn on, integrating N-channel MOSFET power devices to meet high-side load switch applications. The device can operate over an input voltage range of 0.6 V to 5.5 V, and can support a maximum continuous current of 6 A per channel. Each switch is independently controlled by an on and off input (ON1 and ON2), which can interface directly with low-voltage control signals. The RS2581 is capable of thermal shutdown when the junction temperature is above the threshold, turning the switch off. The switch turns on again when the junction temperature stabilizes to a safe range. The RS2581 also offers an optional integrated 220 Ω on-chip load resistor for quick output discharge when the switch is turned off.

The RS2581 is available in a small, space-saving DFN3X2-14 package with integrated thermal pad allowing for high power dissipation. The device is characterized for operation over the free-air temperature range of -40°C to +105°C.

10.2 BIAS Under-voltage Lockout (UVLO)

An under-voltage lockout (UVLO) circuit monitors the BIAS pins voltage to prevent wrong logic controls. The UVLO function initiates a soft-start process after the BIAS supply voltages exceed rising UVLO voltage threshold during powering on.

10.3 Soft-Start

The RS2581 Provides an adjustable soft-start circuitry to control rise rate of the output voltage and limit the current surge during start-up. The soft-start time is set with a capacitor from the CT pin to the ground. (see 10.7 Adjustable Rise Time for more details)

10.4 Enable Control

The ON pin controls the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

10.5 Turn-On & Turn-off the Device

The RS2581 turns on when V_{BIAS}>UVLO & ON=High. **Make sure V_{BIAS} cannot be left floating and must be powered on before VIN. For optimal RON performance, make sure $V_{IN} \leq V_{BIAS}$.** Using ON=Low to turn off the device instead of using V_{BIAS}<UVLO to prevent the ultra-low but unpredictable leakage current which from VIN to OUT result in rising up the OUT voltage.

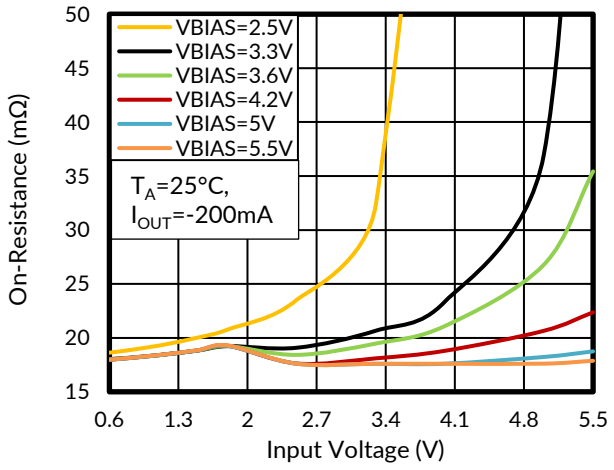

Figure 39. On-Resistance vs Input Voltage (V_{IN}>V_{BIAS} Single Channel)

Preliminary version

10.6 Supply Filter Capacitor

To limit the voltage, drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor, a capacitor needs to be placed between V_{IN} and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high current applications. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

Because of the integrated body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup; however, a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more V_{IN} dip upon turn-on due to inrush currents. This can be mitigated by increasing the capacitance on the C_T pin for a longer rise time (see 10.7 Adjustable Rise Time for more details).

10.7 Adjustable Rise Time

The soft-start capacitor on CT pin can reduce the inrush current and overshoot of output voltage. The soft-start time is set with a capacitor from the CT pin to the ground. The voltage on the CT pin can be as high as V_{BIAS}. The slew rate of VOUT is depended on CT capacitor, the relationship is shown in the equation as below:

SR = 0.406 × CT + 53

SR is the slew rate (in µs/V) from 10% to 90%

CT is the capacitance value on the CT pin (in pF)

The units for the constant 53 are µs/V. The units for the constant 0.406 are µs/(V×pF).

An approximate formula for the relationship between CT and slew rate when V_{BIAS} is set to 5V is shown in Table 1.

Table 1. Rise Time vs CT Capacitor

CT (pF)	Rise Time (µs) 10% - 90%, C_L = 0.1 µF, C_{IN} = 1µF, RL = 10Ω Typical values at 25°C, V_{BIAS}=5V						
	V_{IN} = 5V	V_{IN} = 3.3V	V_{IN} = 1.8V	V_{IN} = 1.5V	V_{IN} = 1.2V	V_{IN} = 1.05V	V_{IN} = 0.6V
0	140	100	70	60	55	50	35
220	460	300	155	130	100	90	50
470	920	600	310	250	195	170	90
1000	1890	1210	650	530	410	350	175
2200	3950	2590	1410	1140	910	775	380
4700	8060	5150	2770	2240	1760	1520	740
10000	16800	11000	6045	4920	3930	3340	1650

10.8 Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0V to the set value. This charge arrives in the from of inrush current. Inrush current can be calculated as follow.

$$\text{Inrush current} = C \times dV/dt$$

Where

C is the output capacitance

dV is the output voltage

dt is the rise time depended on CT capacitance

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10.9 Power Dissipation

The device's junction temperature depends on several factors such as the load, PCB layout, ambient temperature, and package type. Equations that can be used to calculate power dissipation and junction temperature are found below:

$$P_D = R_{DS(ON)} \times I_{OUT}^2$$

To relate this to junction temperature, the following equation can be used:

$$T_J = P_D \times \theta_{JA} + T_A$$

Where:

T_J = junction temperature

T_A = ambient temperature

θ_{JA} = the thermal resistance of the package

11 LAYOUT

11.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for V_{IN}, V_{OUT}, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance. The CT trace must be as short as possible to avoid parasitic capacitance.

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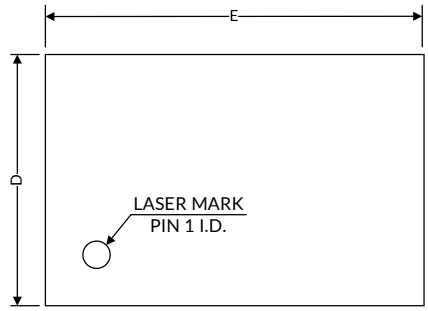
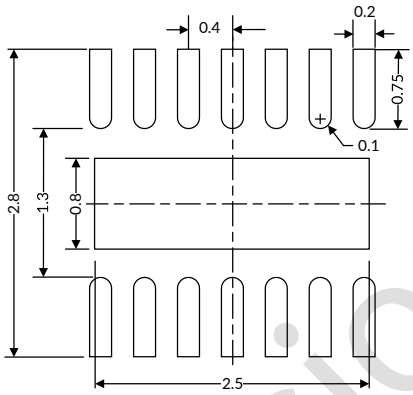
12 PACKAGE OUTLINE DIMENSIONS

DFN3X2-14 (3)

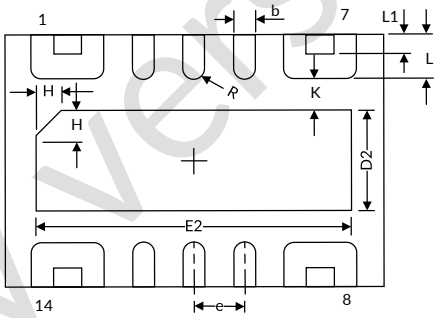


TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)

SIDE VIEW



BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.700	0.800	0.028	0.032
A1	0.000	0.050	0.000	0.002
A3	0.203 REF (2)		0.008 REF (2)	
b	0.130	0.230	0.005	0.009
D (1)	1.950	2.050	0.077	0.081
E (1)	2.950	3.050	0.116	0.120
D2	0.700	0.900	0.028	0.035
E2	2.400	2.600	0.094	0.102
e	0.300	0.500	0.012	0.020
H	0.200 REF (2)		0.008 REF (2)	
K	0.150	-	0.006	-
L	0.300	0.400	0.012	0.016
L1	0.100	0.200	0.004	0.008
R	0.050	-	0.002	-

NOTE:

1. Plastic or metal protrusions of 0.075mm maximum per side are not included.
2. REF is the abbreviation for Reference.
3. This drawing is subject to change without notice.

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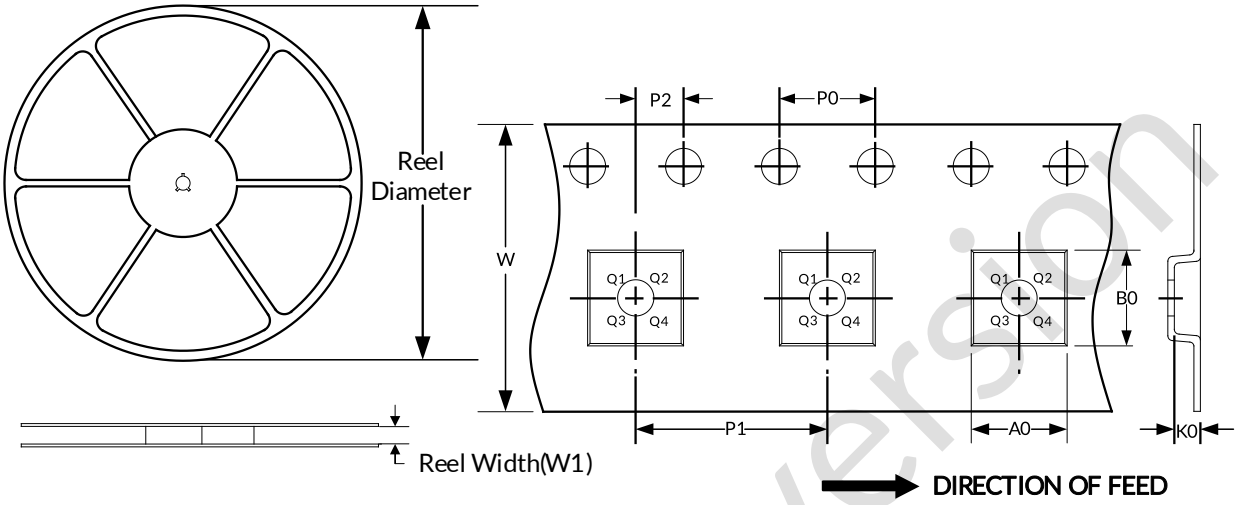
13 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
DFN3X2-14	7”	9.5	3.30	2.30	0.95	4.0	4.0	2.0	8.0	Q2

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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